Radhakrishna Institute of technology & engineering

Subject: Analog Electronics circuit

Semester: 3rd sem

Branch : EE

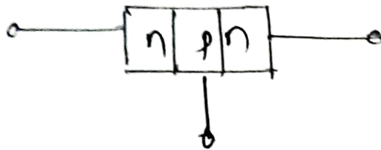
Transistor.

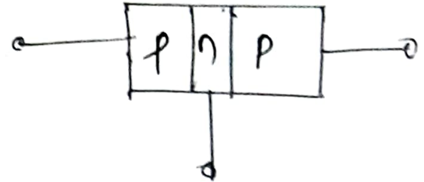
- → Transistor As an amplifier
- → Types
- → Transistor connections
- → characteristics
- → Region of operation.

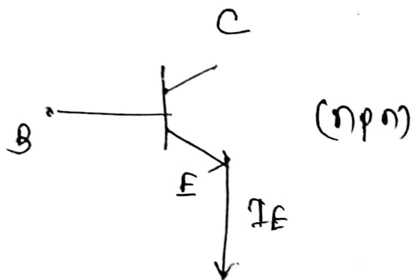
Transfer + Resistor → Transistor

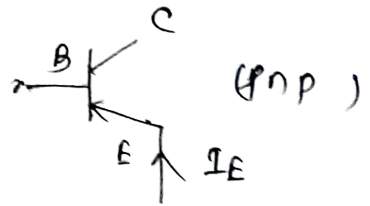
Amplifying action is produced by transferring a current from low resistance → high resistance

Transistor → npn
Transistor → pnp.



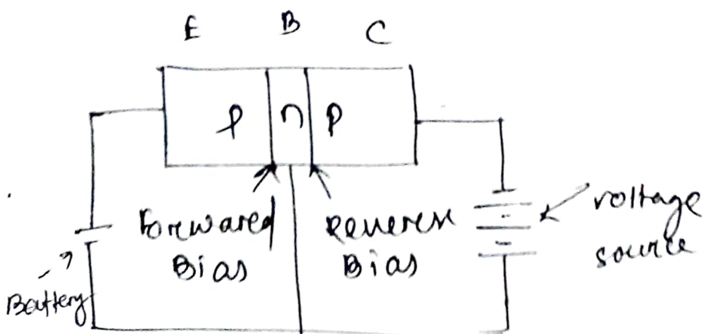


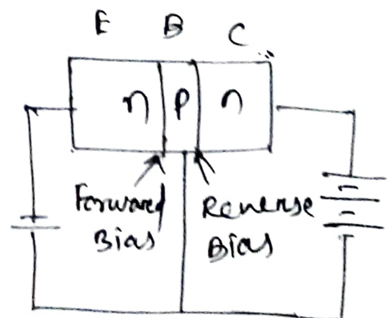




(symbols)

B = Base
C = collector
E = Emitter

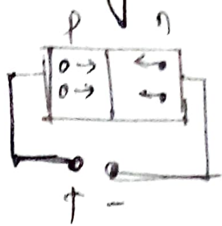




→ The collector (P-type) of a pnp transistor has a reverse bias & receiving hole charges that flow in o/p

The collector (n-type) of npn transistor has reverse bias and received electrons.

→ **Forward Biasing** :- when external voltage applied to the junction is in such a direction that it cancels the potential barrier, thus permitting current flow, called forward biasing.



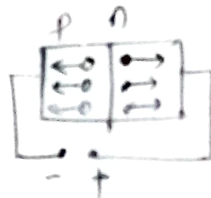
+ve terminal connected → p type

-ve terminal connected → n type

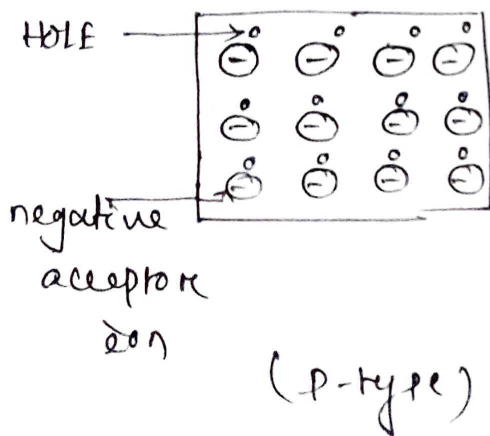
→ **Reverse Biasing** :- when the external voltage applied to the junction is in such a direction that potential barrier is increased, it is called reverse biasing.

-ve terminal → p type

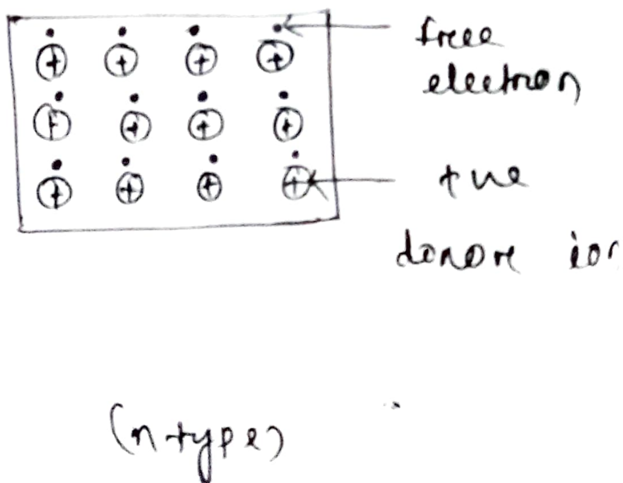
+ve " → n type



→ **Properties of pn junction** :-



(p-type)



(n-type)

→ in p-type current carried by holes.

→ in n-type current carried by free electron.

→ The -ve terminal when connected to n type, it repels free electrons in n type

Transistor connections.

→ 3 leads in transistor:

- collector
- Base
- Emitter.

→ But for connection, 4 terminals require.

- 2 for i/p.
- 2 for o/p

→ This problem overcome by making one terminal common to both output and input.

→

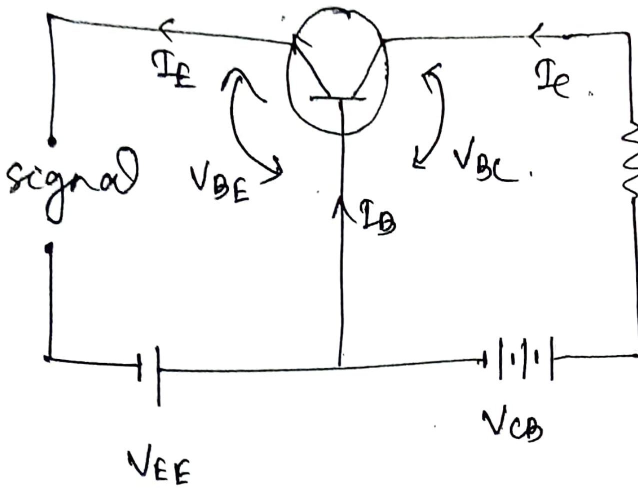
Transistor connection

- Common Base Connection
- Common Emitter connection
- Common collector Connection

characteristics	Common Base Connection	Common Emitter connection	Common collector Connection
1. Input Resistance	Low (100 Ω)	Low (750 Ω)	Very high (750 KΩ)
2. O/P Resistance	very High (450 KΩ)	High (45 KΩ)	Low (50 Ω)
3. voltage gain	150	500	less than 1
4. Application	for high frequency applications	for audio frequency applications	for impedance matching

Common Base Connection

I/P applied between emitter & Base.
O/P taken from collector & Base.

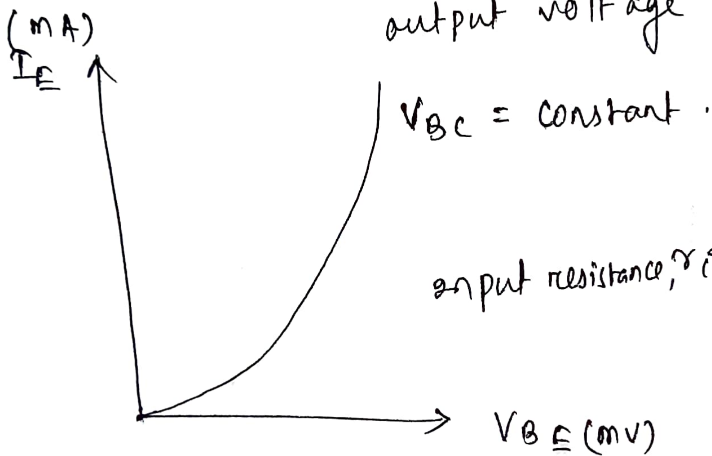


current amplification factor

$$\alpha = \frac{\Delta I_C}{\Delta I_E}$$

Input characteristics

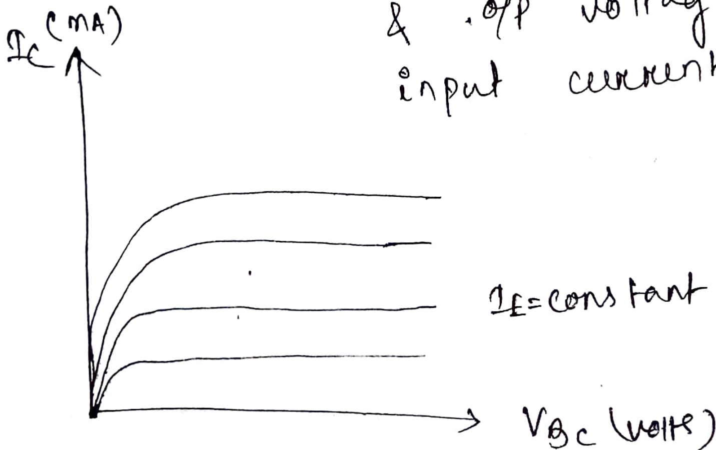
Graph is in between input current and input voltage when output voltage is constant.



input resistance, $r_i = \frac{\Delta V_{BE}}{\Delta I_E}$

Output characteristics

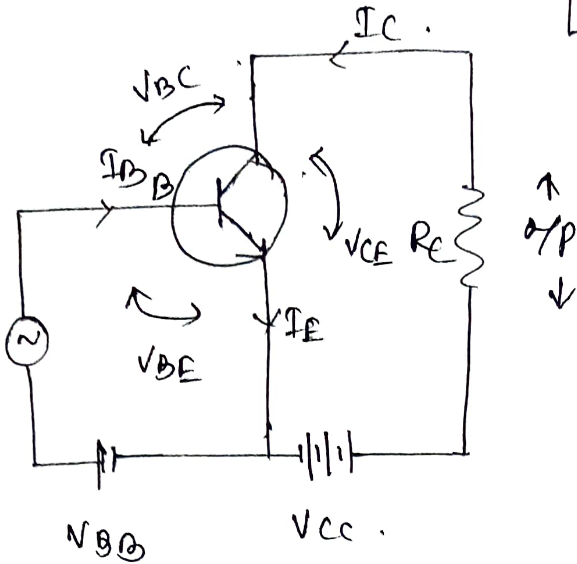
Graph is inbetween o/p current & o/p voltage where input current is constant



output resistance, $r_o = \frac{\Delta V_{BC}}{\Delta I_C}$

Common Emitter connection

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$



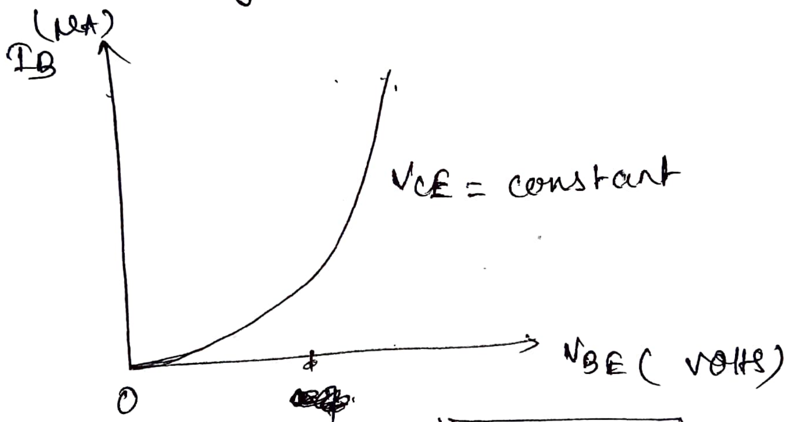
$I_B \rightarrow$ input current

$I_C \rightarrow$ o/p "

$V_{BE} \rightarrow$ i/p voltage

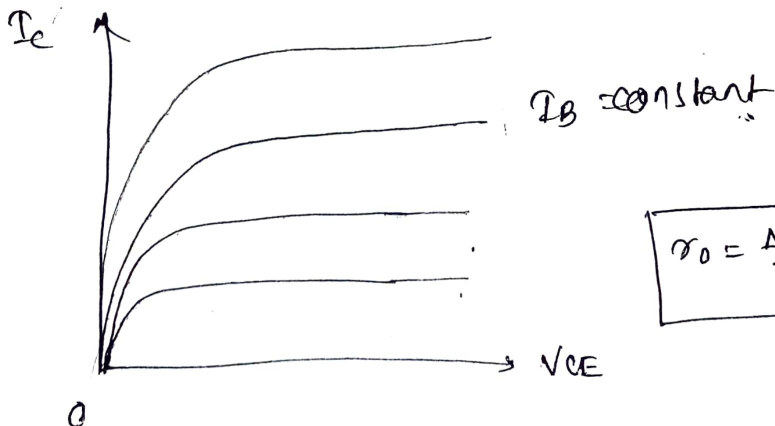
$V_{CE} \rightarrow$ o/p voltage.

Input characteristics. It is the curve between base current I_B & base-emitter voltage V_{BE} at constant collector-emitter voltage V_{CE}.



$$r_i = \frac{\Delta V_{BE}}{\Delta I_B}$$

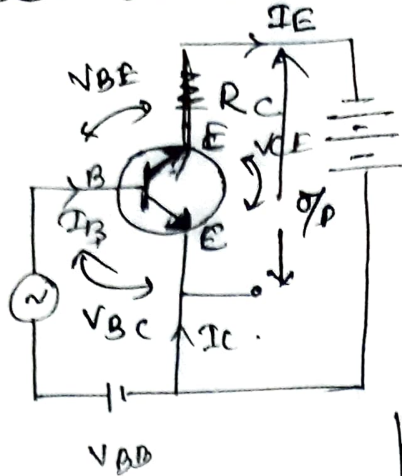
output characteristics

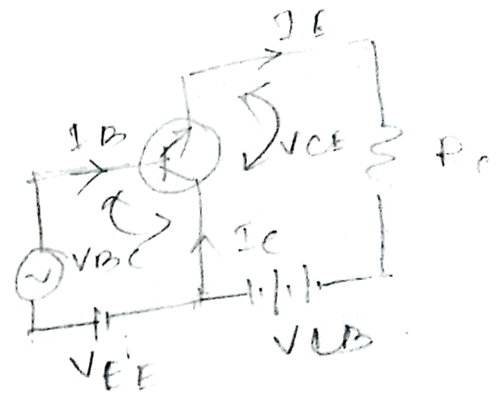


$$r_o = \frac{\Delta V_{CE}}{\Delta I_C}$$

Graph is in between output current & output voltage where input current remains constant.

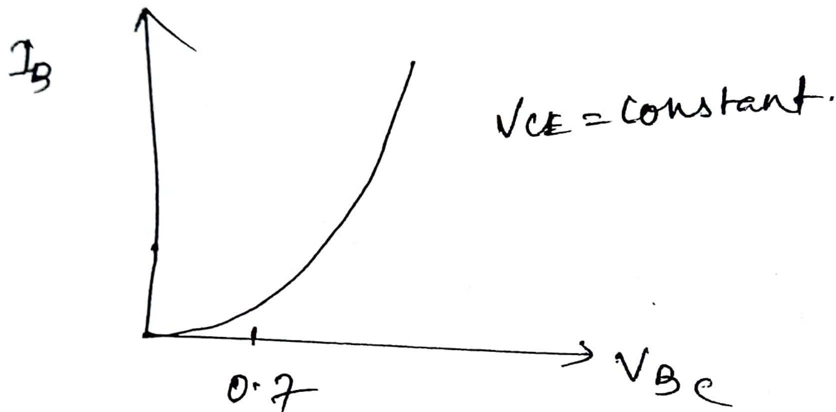
common collector connection



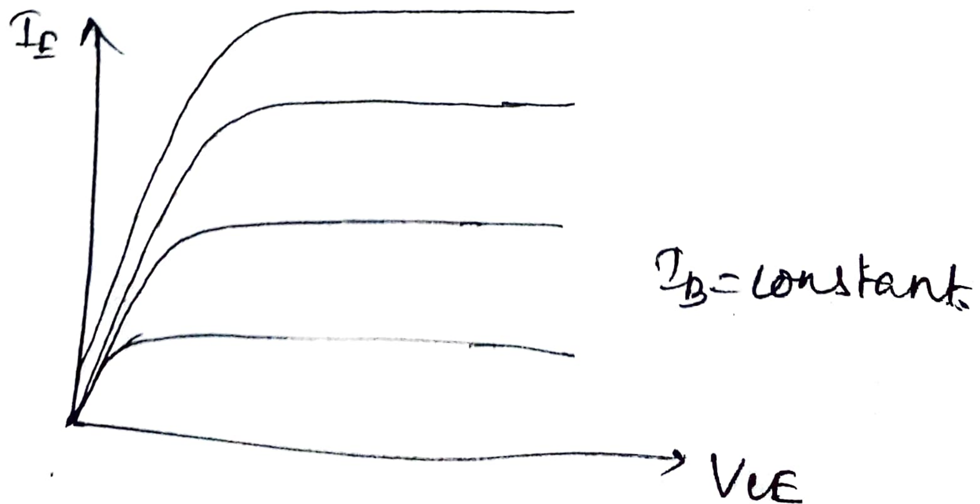


$$\gamma = \frac{\Delta I_E}{\Delta I_B} = \frac{\text{change in emitter current}}{\text{change in base current}}$$

input characteristics



output characteristics



Load Line

collector-emitter voltage $V_{CE} = V_{CC} - I_C R_C$.

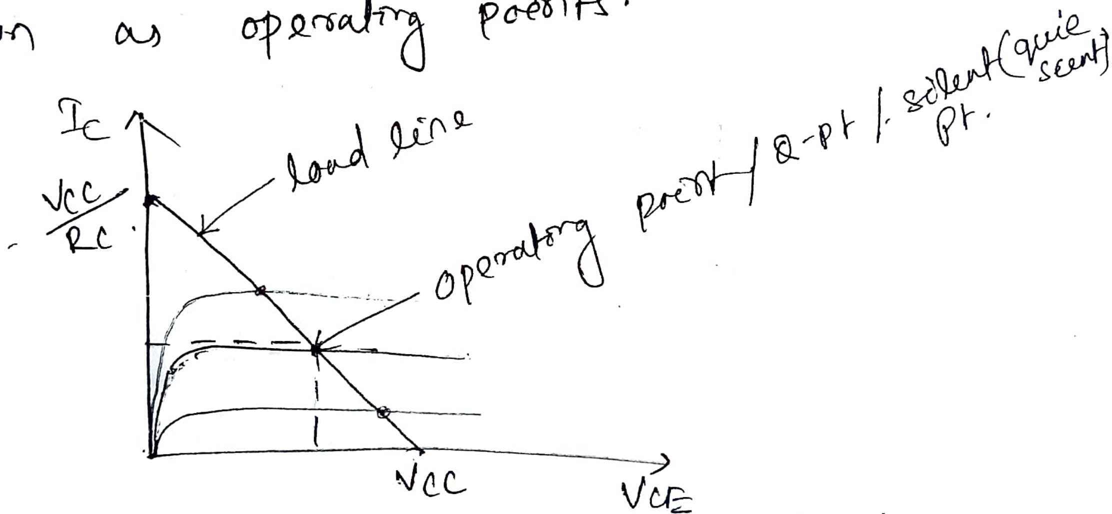
As V_{CC} & R_C are fixed values, therefore, it is a first degree equation and can be represented by a straight line on the output characteristics. This is known as d.c. load line & determines the locus of $V_{CE} - I_C$ points for any given value of R_C.

max $V_{CE} = V_{CC}$

max $I_C = \frac{V_{CC}}{R_C}$.

operating point

The zero signal values of I_C & V_{CE} are known as operating points.

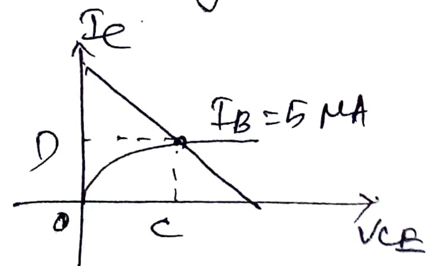


It is the intersection between the load line & the output characteristics of a transistor.

→ It is called Q.pt b'coz it is the pt on $I_C - V_{CE}$ characteristic when the transistor is silent i.e in the absence of the signal.

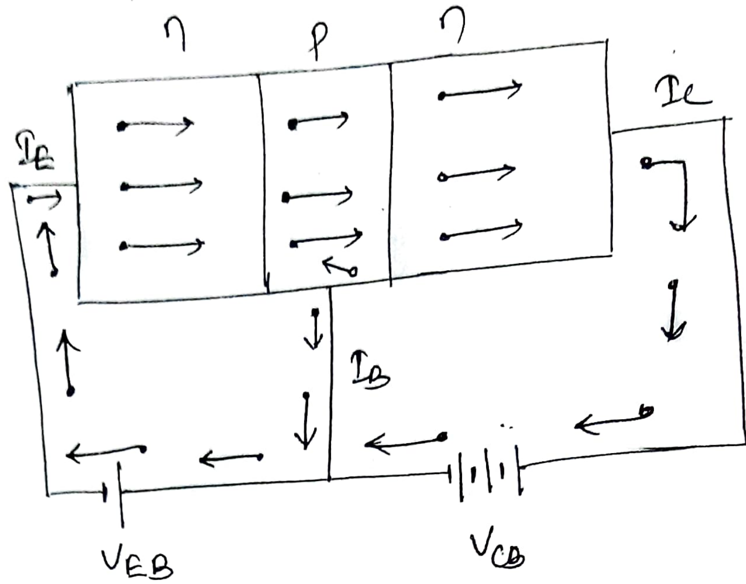
$V_{CE} = OC$ volts

$I_C = OD$ mA.



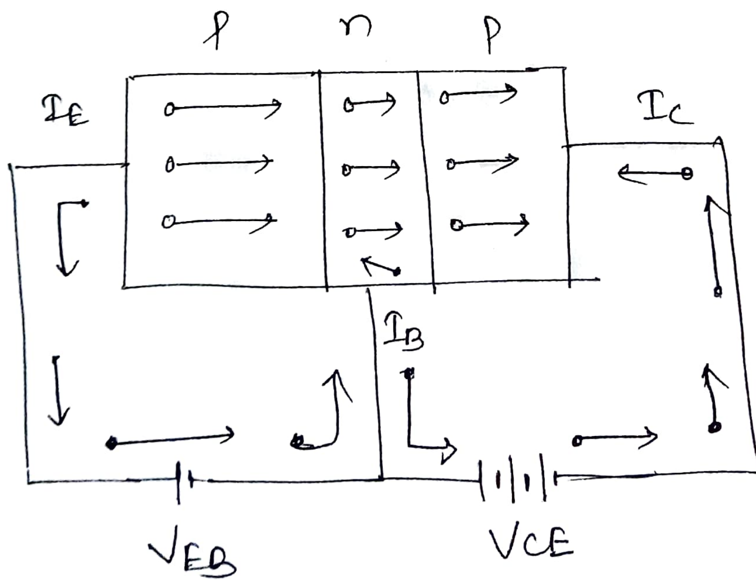
Working

npn transistor



(Basic connection of npn)

pnp transistor



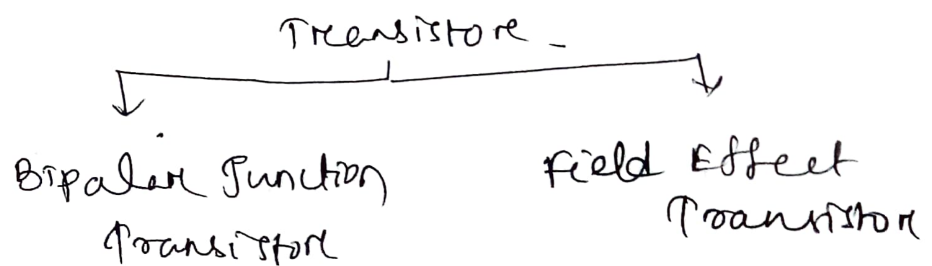
2 types of current in pn junction. — Diffu[sion] / Drif[t]

Diffusion current

Diffusion current is due to the flow of the maxm concentration of charge carriers in a pn junction.

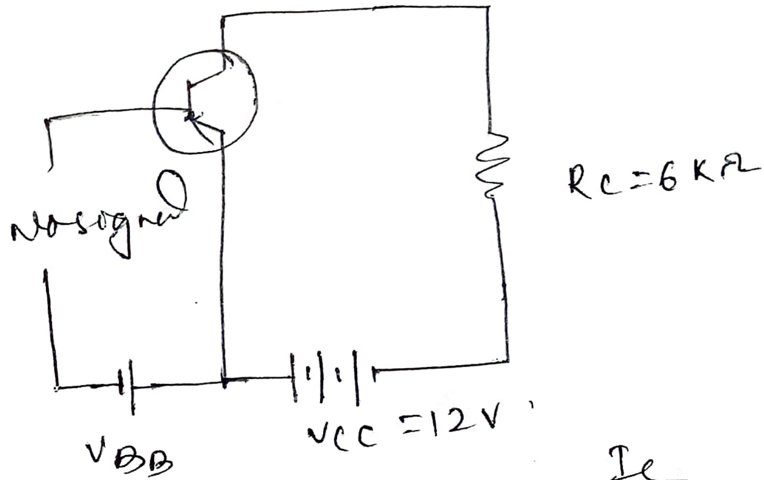
Drift current

This current is due to the movement of majority charge carriers in a pn-junction on the application of an external voltage supply.



- Bipolar represents the flow of both the charge carriers i.e electrons & holes.
- Field represents that the electric current flow is due to the ~~characteristics~~ creation of electric field in FET.
- FET is an unipolar device that means the current flows is due to the movement of single charge carriers (either electron or holes.

Q.2 Draw the d.c load line & what will be the Q.pt of zero signal base current is 20μA & $\beta = 50$.



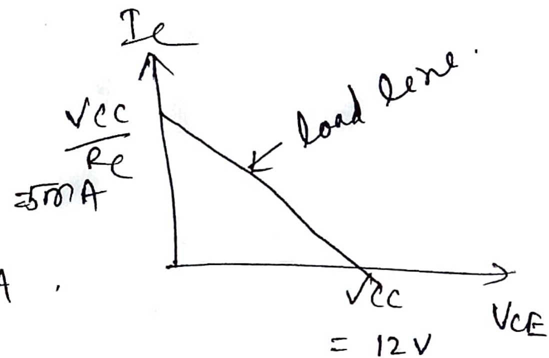
Sol^n

Load line

$V_{CE\,max} = V_{CC}$

$= 12V$

$I_{C\,max} = \frac{V_{CC}}{R_C} = \frac{12}{6\times10^3} = 5\,mA$



Q.pt

$V_{CEQ} = V_{CC} - I_C R_C$

$= 12V - (\beta I_B) R_C$

$= 12V - (50 \times 20\times10^{-6}) \cdot R_C$

$= 12 - 1\,mA \cdot R_C$

$= 12 - (1\times10^{-3}) \times (6\times10^3)$

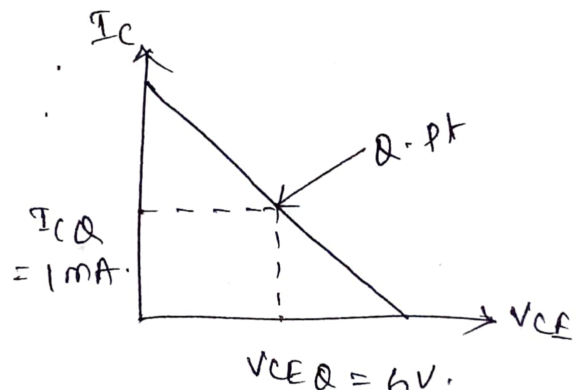
$= 6\,V$

$I_{CQ} = \beta I_B$

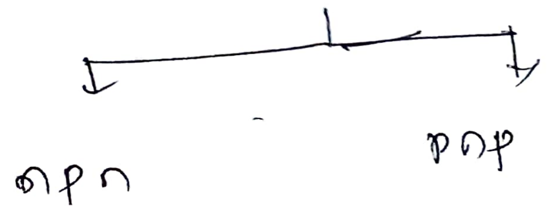
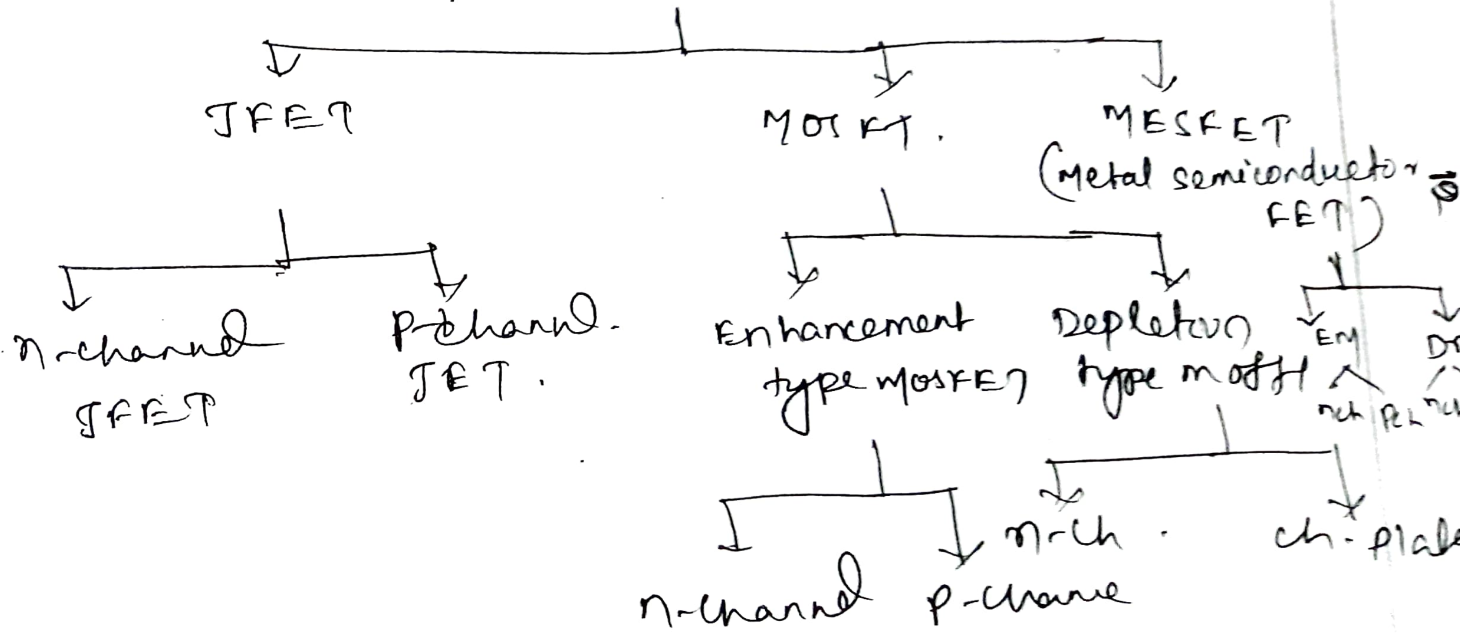
$= 50 \times 20\,\mu A$

$= 50 \times 20 \times 10^{-6}$

$= 1\,mA$



Classification of Transistors

MODULE - I

FIELD EFFECT TRANSISTOR

The FET is a three-terminal device used for a variety of applications.

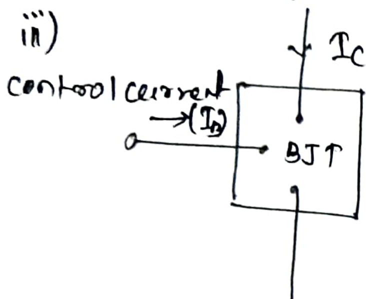
Difference Between BJT & FET

BJT

i) BJT transistor is a current-controlled device.

ii) output characteristics of the device are controlled by base current & not by base voltage.

iii)



(a)

The current I_C in fig(a) is a direct function of the level of I_B.

iv) BJT transistor are two types.
- npn bipolar transistor
- pnp " "

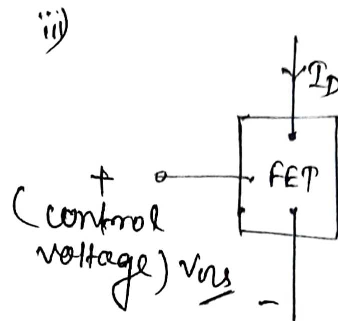
v) BJT is a bipolar device where bi indicates that the conduction levels is a ... of ... charge carriers (electrons & holes)

FET

i) JFET transistor is a voltage-controlled device.

ii) In FET, the output characteristics are controlled by input voltage (i.e electric field) & not by input current.

iii)



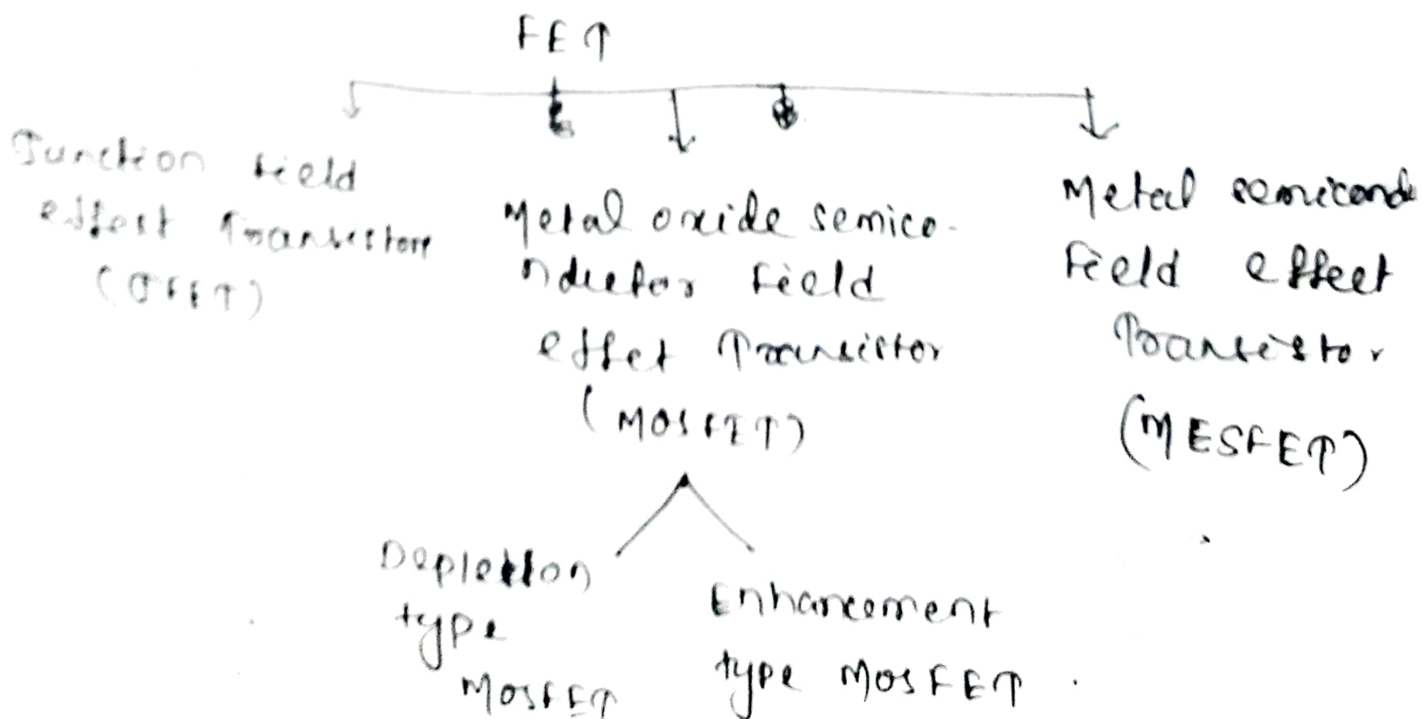
(b)

The current I_D will be a function of the voltage V_{GS} applied to the input circuit of fig(b).

iv) FET transistor can be
- n-channel transistor
- p-channel "

v) FET is a unipolar device depending on either electron (n-channel) or hole (p-channel) conduction.

BJT	FET
vi) BJT has low i/p impedance.	vi) FET has high input impedance.
vii) voltage gain for BJT amplifiers are more.	vii) ~~FET~~ voltage gain for FET amplifiers are less.
viii) BJT are ~~not~~ less temperature stable	viii) FET are more temperature stable.
ix) BJT are larger in size.	x) FET are smaller than BJT. so useful in integrated circuit chip.

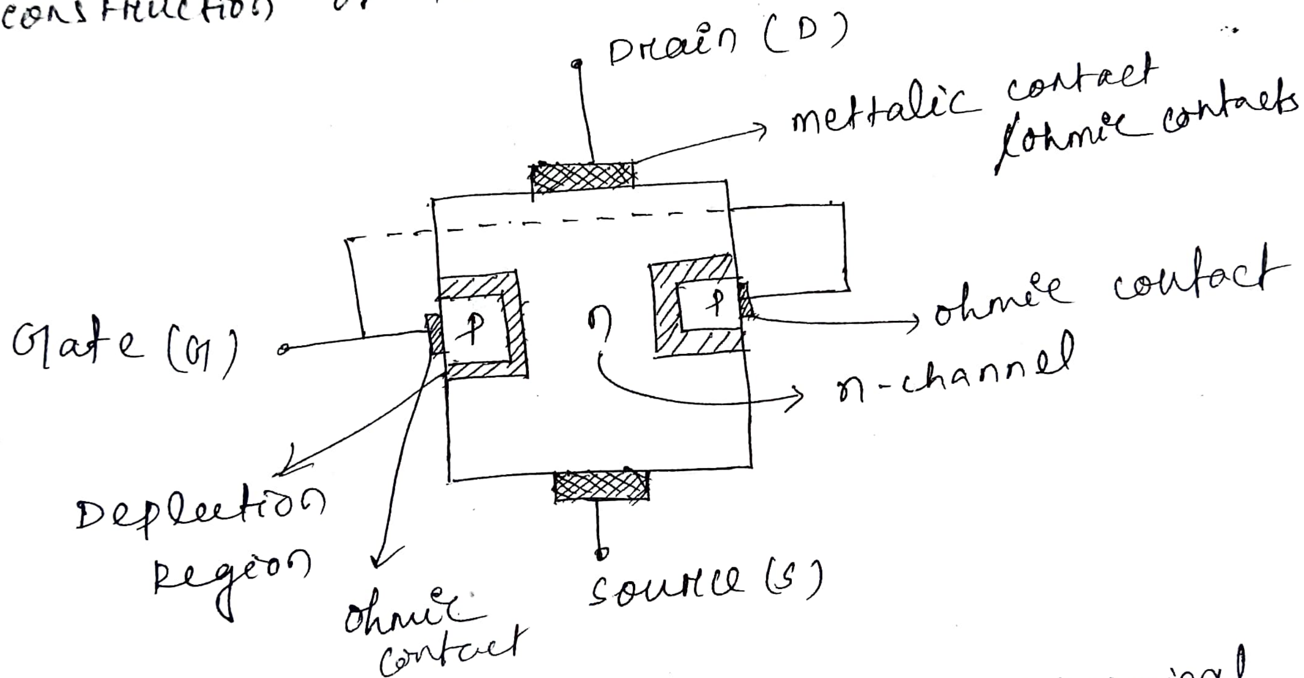


Why the name Field Effect Transistor

For FET electric field is established by the charges present that controls the conduction of the output circuit without the need for the direct contact between controlling and controlled quantities.

Construction of JFET.

Construction of n-channel JFET :-



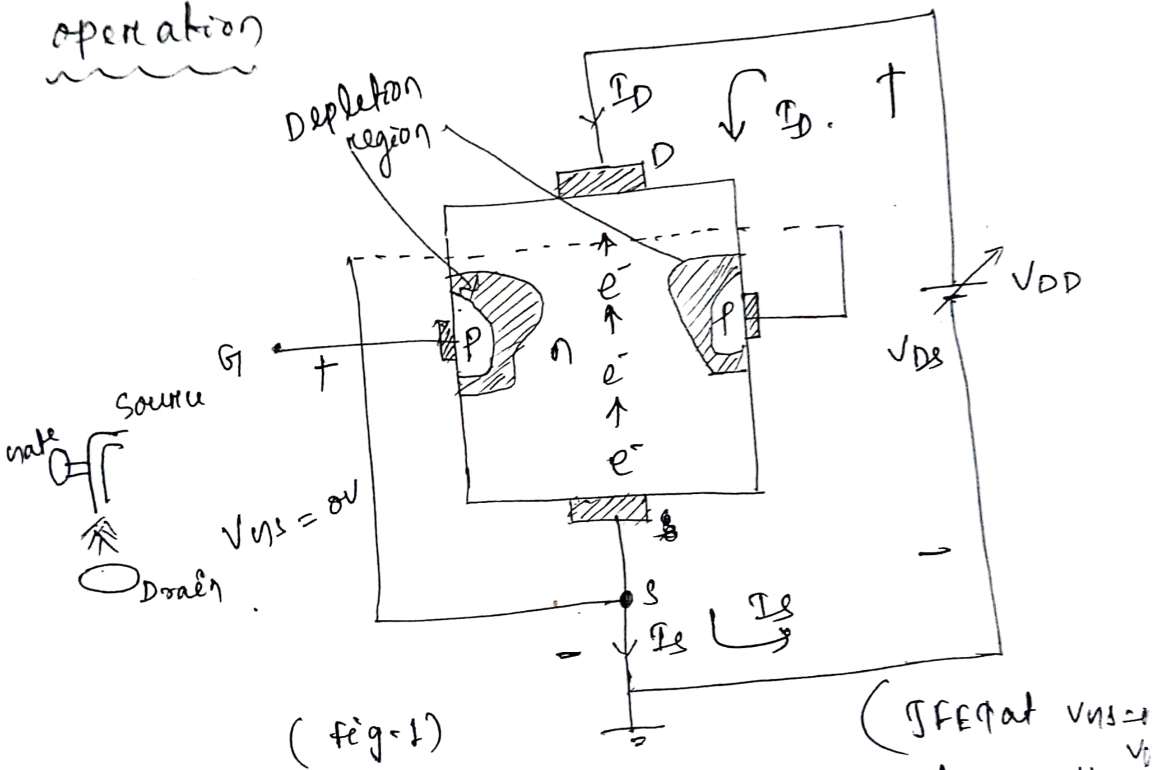
→ It is a 3 terminal device with 1 terminal capable of controlling the current between the other two.

→ For a n-channel JFET major part of the structure is n type that forms the channel. between embeded layer of the 2 p-type materials.

→ The top of n-channel is connect through mettalic contact to the terminal referred to as drain while the lower end of the same material is connected to a terminal refered to as source.

→ The two p-type materials are connected together to the gate terminal.

operation



(fig-1) (JFET at $V_{GS}=0$ V)

- On the absence of any applied voltage, JFET has two pn junctions as a result of which there is a depletion region at each of a junction.

- Due to the application of voltage from drain to source the current is establ[ished] from the source. The "gate", through an applied potential controls the flow of charge to the drain.

Case-1 (Fig-2)

$V_{GS} = 0V$, V_{DS} = some +ve value.

- The result is the gate and a source terminal at the same potential & a depletion region in the lower end of each p-type material similar to the no bias condition.

- The instant voltage $V_{DS} = V_{DD}$ is applied, electrons are drawn to the drain terminal establishing current I_D drain terminal.

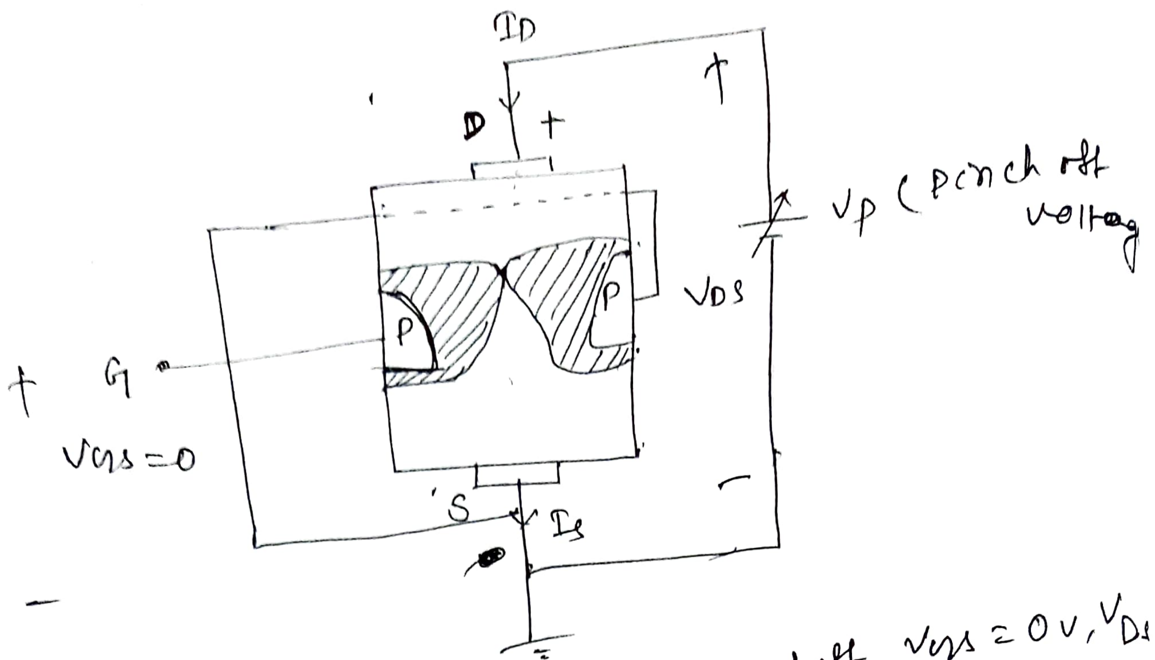
$$I_D = I_S$$

- The region for change in width of the depletion region is due to the fact that different voltage level are set up by the drain current due to non-uniform distribution of resistance in the n-channel.

- Hence the upper region is more reverse biased compared to the lower.

- If V_{DS} ~~is foo~~ increased from 0 → few volts, current will increase.

N.B. Forward Bias junction has low resistance path & vice versa.



(Fig-2) (pinchoff $V_{GS} = 0V$, V_{DS}

- As V_{DS} increases and approaches the value equal to V_P, then depletion regions will widen causing a reduction in a n-channel

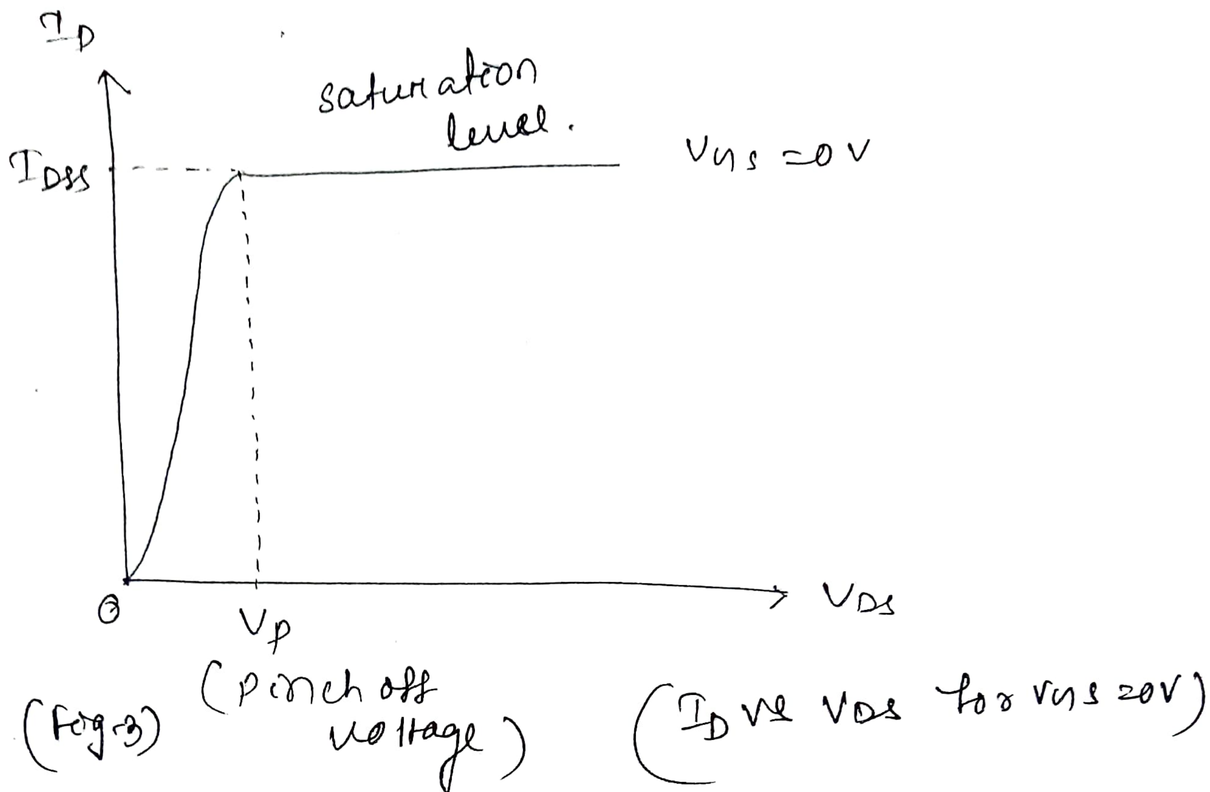
- At this point of time when the two depletion region touch each other, the condition is reffered to as pinch-off & the voltage is known as pinch off voltage.

- when V_{DS} increases beyond V_P, the region between the depletion region increases in length but I_D remains same and denoted as I_{DSS}.

- I_{DSS} is the maximum current for JFET & defined by the condition $V_{GS} = 0V$.

$$V_{DS} > |V_P|$$

characteristics.



(Fig-3) (I_D vs V_{DS} for $V_{GS} = 0V$)

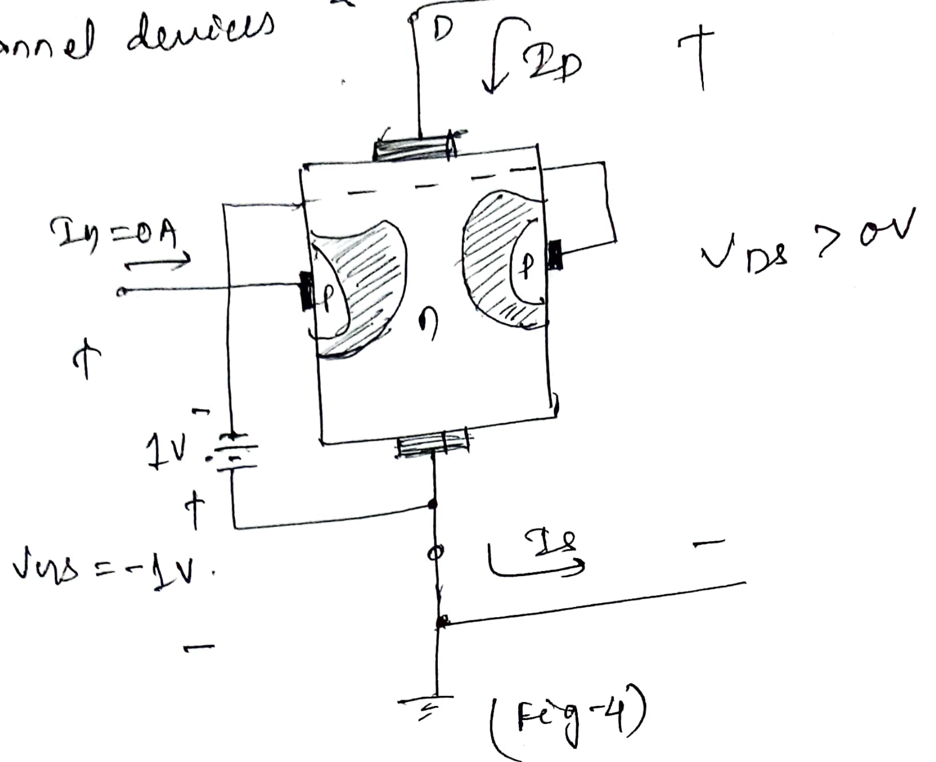
case-2 (Fig-4)

- A voltage of -1V is applied between gate and source, the current reaches the saturation level earlier as compared to $V_{GS} = 0V$ condition.
- Hence the saturation level will be met at the lower value of V_{DS}.
- when V_{GS} is made more negative i.e equal to $-V_p$. It is sufficiently negative to establish 0mA and the device gets turned off.

Pinch off voltage – It is the minimum drain-source voltage at which the drain current essentially becomes constant.

is defi[ned]

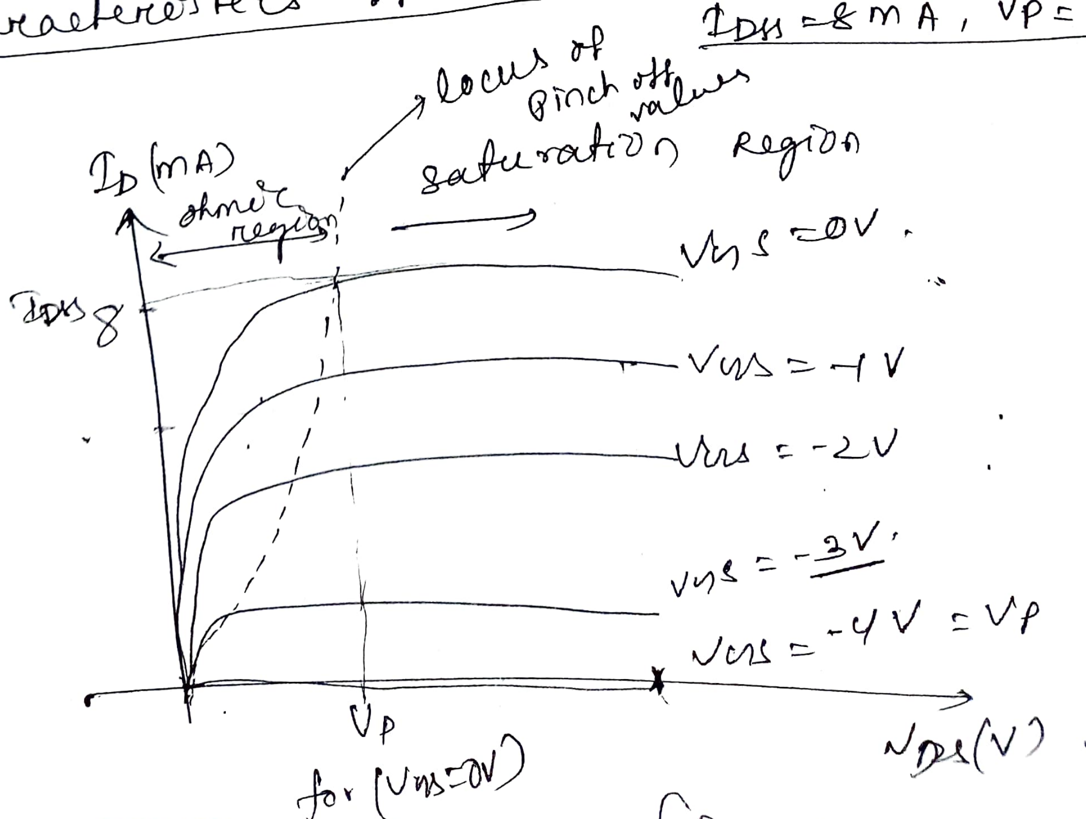
→ The level of V_{GS} that results in $I_D = 0\,mA$ is defined by $V_{GS} = V_P$, with V_P being a −ve voltage for n channel devices & +ve value for p-channel de[vices].



(Fig-4)

(Application of a negative voltage to the gate of a JFET)

characteristics of n channel JFET with $I_{DSS} = 8\,mA$, $V_P = -$[4V]

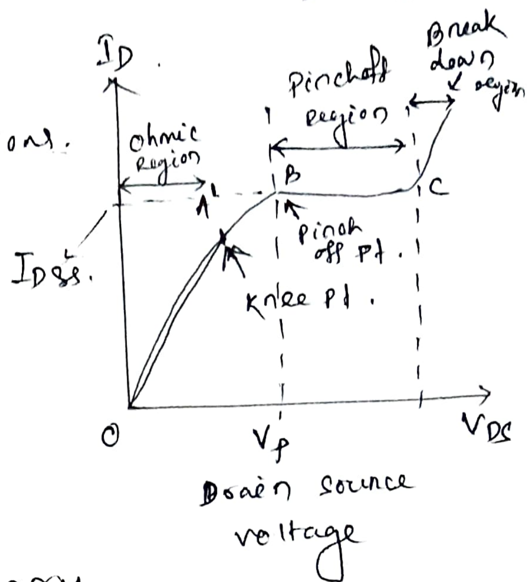


Characteristics of a JFET

- 2 types of characteristics. 1) output / Drain characteristics
  2) Transfer characteristics.

(1) Drain characteristics :- It gives relation between I_D & V_{DS} for different values of V_{GS}.

- It can be subdivided into 4 regions.



1) Ohmic Region (OA) -

- During this period the curve is linear for low values of V_{DS}.
- current varies directly with voltage following ohm's law.
  i.e JFET behaves like an ordinary resistor till pt. "A" called knee point.

2) Curve (AB) :- I_D increases at a very low rate upto pt B. i.e from pt "A" to pt "B".

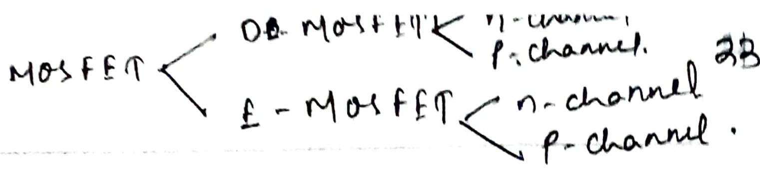
- V_{DS} corresponding to pt "B" called pinchoff voltage.

3) Pinch off Region (BC) :- It is known as saturation or amplified region.

- During this period V_{DS} increases but I_D remains constant & named as I_{DSS}.
- During this period no external bias required as $V_{GS} = 0V$.

4) Break down region ~~Drain current region~~ **:-** If V_{DS} increases beyond the saturation value, then I_D increases rapidly.

- Bcoz the reverse biased gate channel PN junction undergoes Avalanche breakdown.



↳ DEPLETION TYPE MOSFET / DE MOSFET.

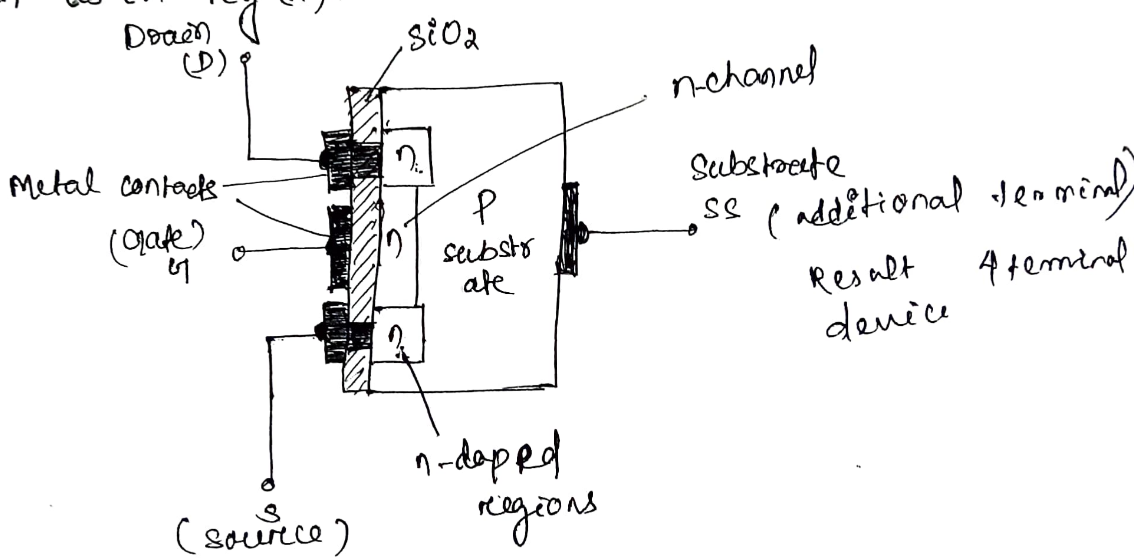
Basic construction · By changing the polarity of V_{GS}, it can operate in both mode.

→ A slab of p-type material is formed from a silicon base & is referred to as the substrate.

→ It is the foundation on which the device is constructed.

→ The substrate is internally connected to the source terminal.

→ Many discrete device provide an additional terminal labeled SS, resulting in a four-terminal device, such as in fig (a).



→ The source & drain terminals are connected through metallic contacts to n-doped regions linked by an n-channel as shown in fig.

→ The gate is also connected to a metal contact surface but remains insulated from the n-channel by a very thin silicon dioxide (SiO_2) layer.

→ SiO_2 is a type of insulator referred to as a dielectric, which sets up opposing electric fields with dielectric when exposed to an externally applied field.

* SiO_2 layer is an insulating layer means that:
→ There is no direct electrical connection betn the gate terminal & the channel of a MOSFET
→ It is the insulating layer of SiO_2 in the MOSFET construction that accounts for the very desirable high i/p impedance of the device.
so $I_G = 0$
→ The input resistance of a MOSFET is more than that of a typical JFET, even though the input impedance of most JFETs is sufficiently high for most applications.

→ B'coz of high i/p impedance $I_G = 0A$ for dc bias configuration.

→ In MOSFET
- Metal for drain, source & gate
- oxide for silicon dioxide insulating layer.
- semiconductor for the basic structure on which the n-and p-type regions are diffused.

→ The insulating layer between the gate and the channel has resulted in another name for the device : insulated-gate FET, or IGFET.

BASIC OPERATION AND CHARACTERISTICS

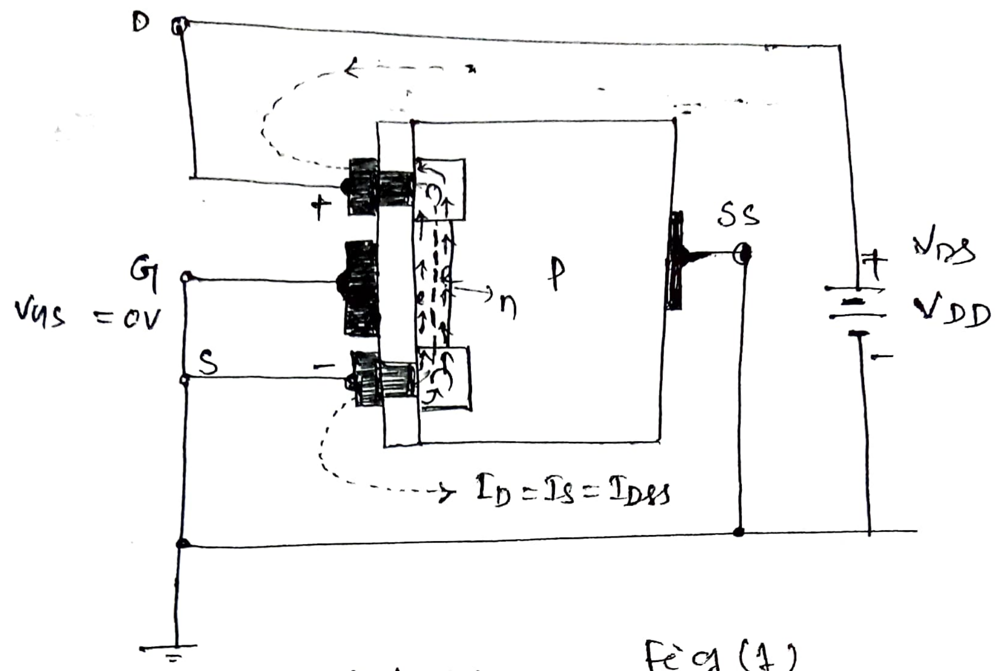


Fig (1)
~~n-type~~ n-channel depletion-type MOSFET with $V_{GS} = 0V$ & applied voltage V_{DD}.

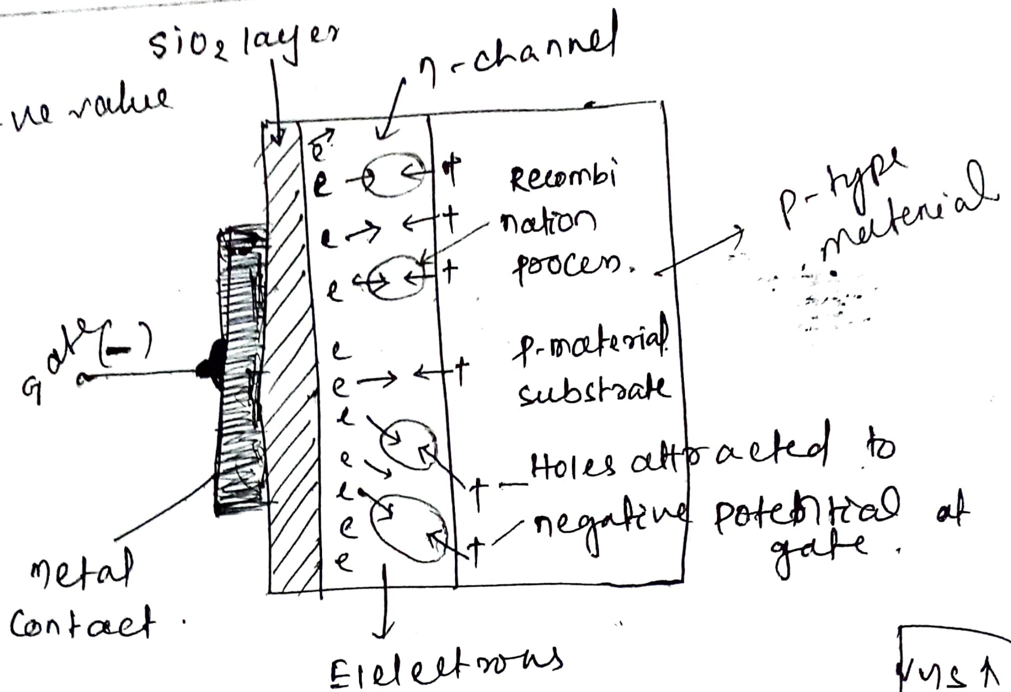
Case - I $V_{GS} = 0V$, V_{DS} = +ve value

→ The gate & source voltage is set to 0V by the direct connection from one terminal to the other & a voltage V_{DS} is applied across the drain-to-source terminals.

→ The result is an attraction for the positive potential at the drain by the free electrons of the n-channel and a current similar to that established through the channel of the JFET.

Case - II

V_{GS} = -ve value



(fig-3)

Reduction in free ~~electrons~~ carriers in a channel due to a negative potential at the gate terminal.

→ V_{GS} is set at negative voltage such as -1V.

→ The -ve potential at the gate will tend to pressure electrons toward p-type substrate (like charges repel) & ~~holes~~ attracts holes from the p-type substrate (opposite charges attract) as shown in the above figure.

→ Depending on the magnitude of the negative bias established by V_{GS}, a level of recombination between electrons & holes will occur that will reduce the number of free electrons in the n-channel available for conduction.

→ The more negative the bias, the higher is the rate of recombination.

→ The resulting level of drain current is therefore reduced with increasing negative bias for V_{GS}.

Case - III V_{GS} = +ve value, the +ve gate will draw the addition electrons (minority carrier) from p-type material.

→ If we apply $V_{GS} = 4V$ then

$I_D = 22.2 mA$.

→ If V_{GS} increase I_D increase at a rapid rate.

That means I_D exceed the maximum rating (current or power) for the device.

| $V_{GS} \uparrow$ $I_D \uparrow$ |

→ The application of a positive gate-to-source voltage has "enhanced" the level of free carriers in the channel compared to that encountered with $V_{GS} = 0V$.

→ So region of positive gate voltages on the drain/transfer characteristics is often reffered to as the enhancement region.

→ The region betn cutoff & saturation level of I_{DSS} referred to as the depletion region.

→ The relationship betn I_D & V_{GS} is defined by shockley's equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Control variable → V_{GS}

Constants → I_{DSS}, V_P

$$I_D = \begin{cases} I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 & V_{GS} > V_P \text{ (n-channel)} \\ & V_{GS} < V_P \text{ (p-channel)} \\ 0 & \text{otherwise} \end{cases}$$

Transfer characteristics :-

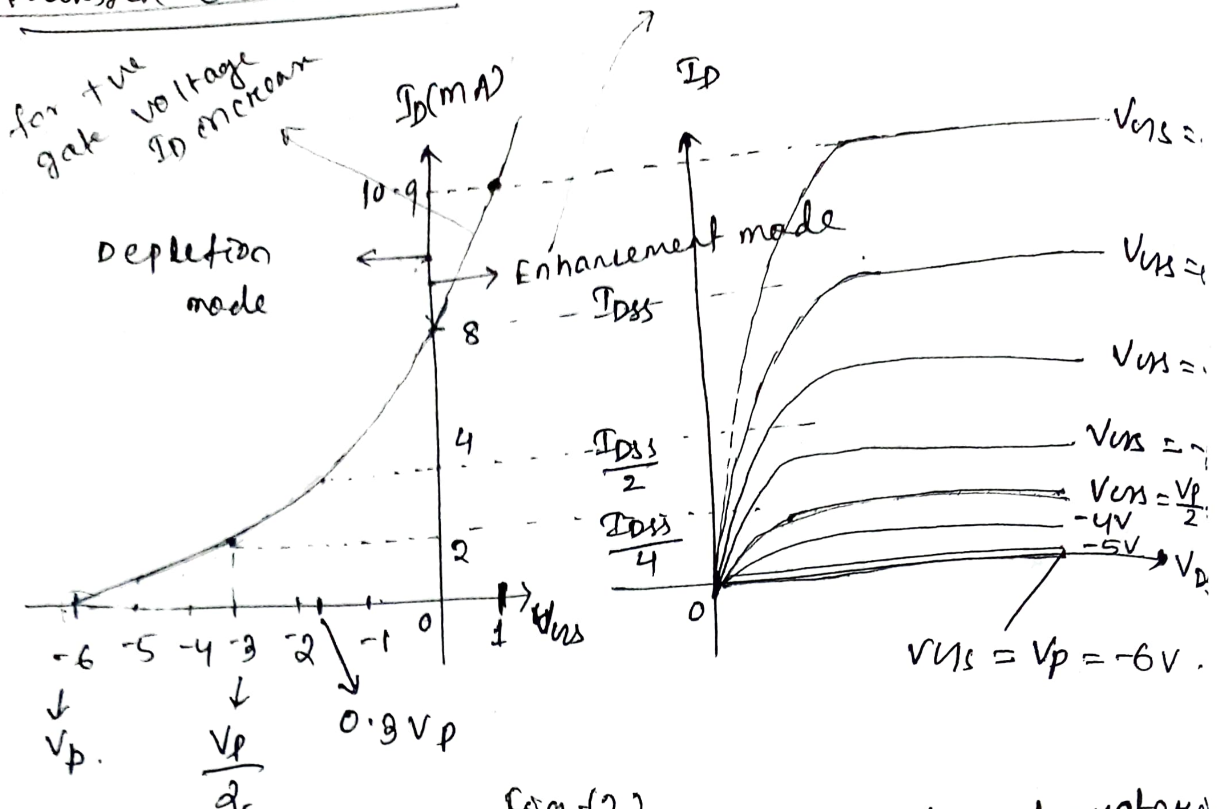


Fig-(2)

Drain characteristic & Transfer characteristic for an n-channel depletion MOSFET.

From above figure :-

i) I_{DSS} (shorted-gate drain current) :- It is the drain current with source short-circuited to gate (i.e $V_{GS} = 0$) and drain voltage (V_{DS}) equal to pinch off voltage. It is some times called zero-bias current.

ii) V_{DS} - ~~Maximum~~ drain to source voltage

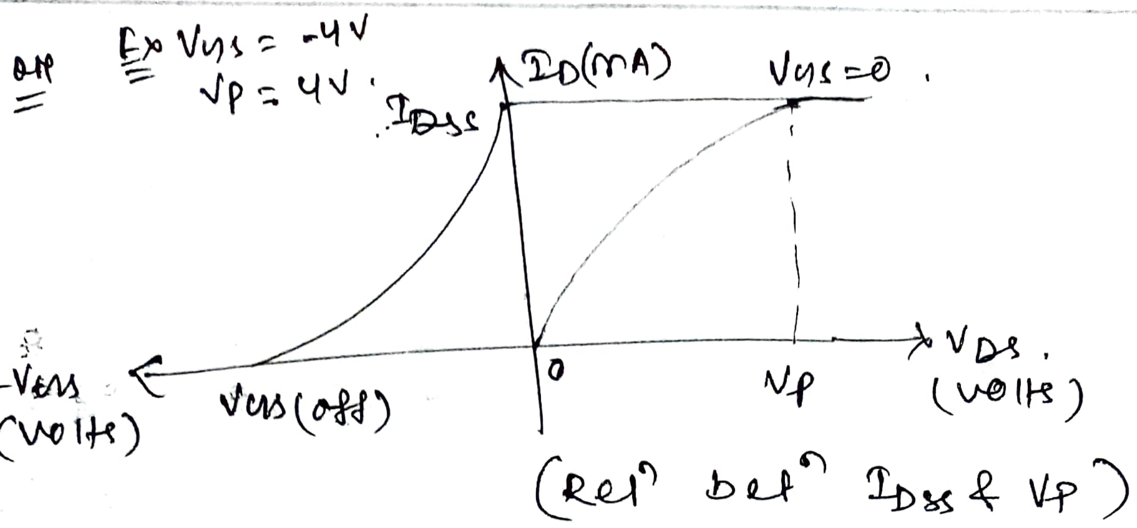
iii) V_{GS} - Gate to source voltage

iv) I_D - drain current

v) V_P (pinch off voltage) - It is the minimum drain source voltage at which the drain current essentially becomes constant.

If $V_{DS} > V_P$ → then JFET can operate.

If $V_{DS} > V_{DS(max)}$ → then JFET breakdown.



(Relⁿ betⁿ I_{DSS} & V_P)

Expression for drain current I_D :-

$V_{GS(off)}$ → Gate-source cut off voltage : It is the gate-source voltage where the channel is completely cut off and the drain current becomes zero.

$V_P = V_{GS(off)}$ (∵ By drain characteristic)

so
$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

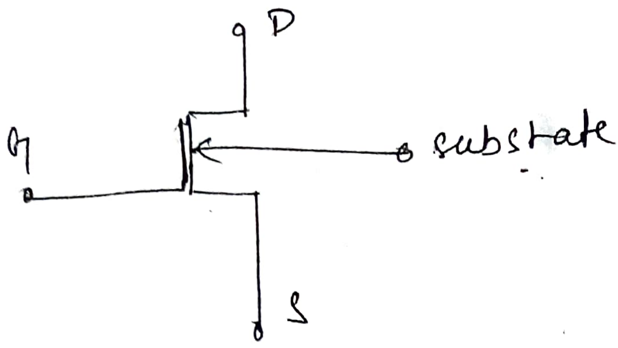
I_D = drain current at given V_{GS}.

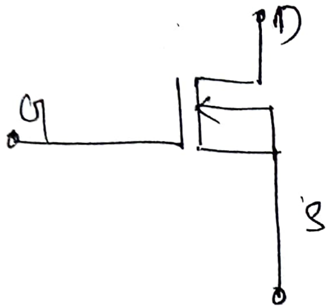
I_{DSS} = Shorted - gate drain current

V_{GS} = gate - source voltage.

$V_{GS(off)}$ = gate - source cut off voltage.

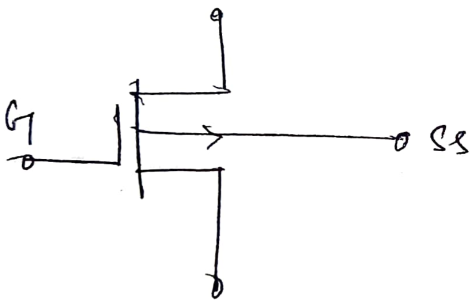
symbol

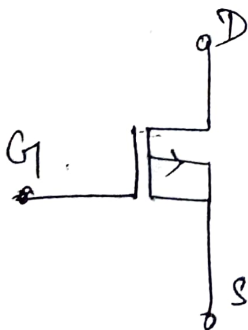




substrate connected to soun

(n-channel depletion-type mosfet)





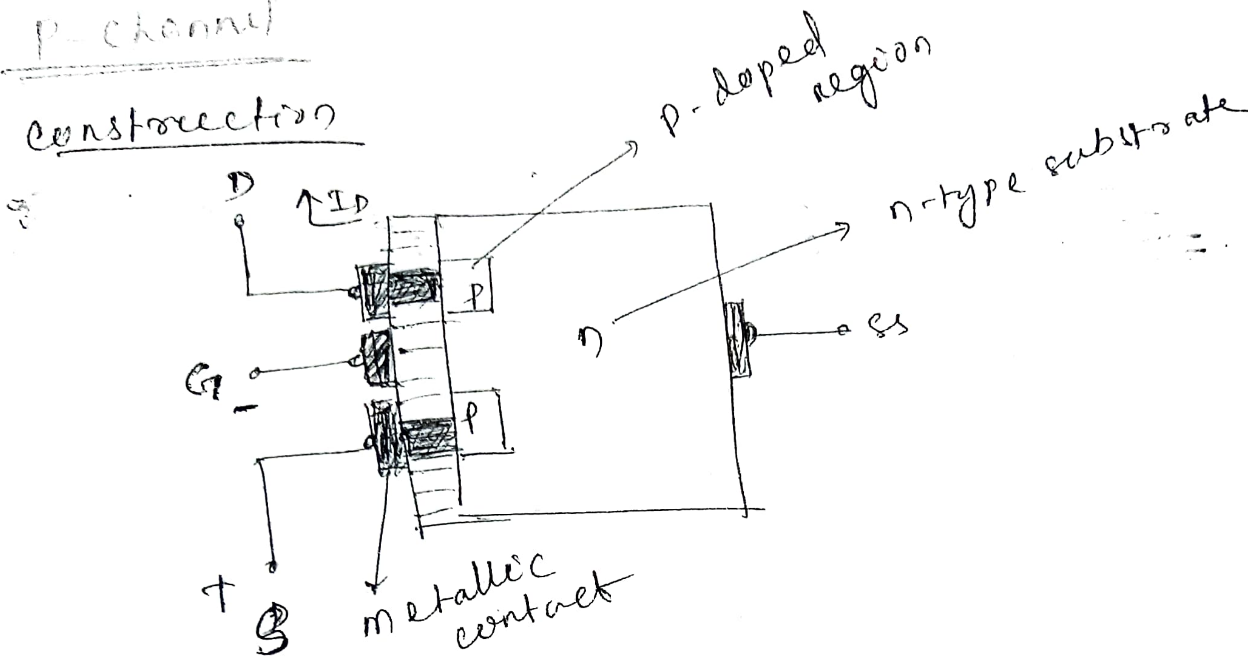
(p-channel depletion-type Mosfet)

Module - I (MOS field effect Transistor)
chapter - 1

Enhancement type MOSFET

p channel

construction

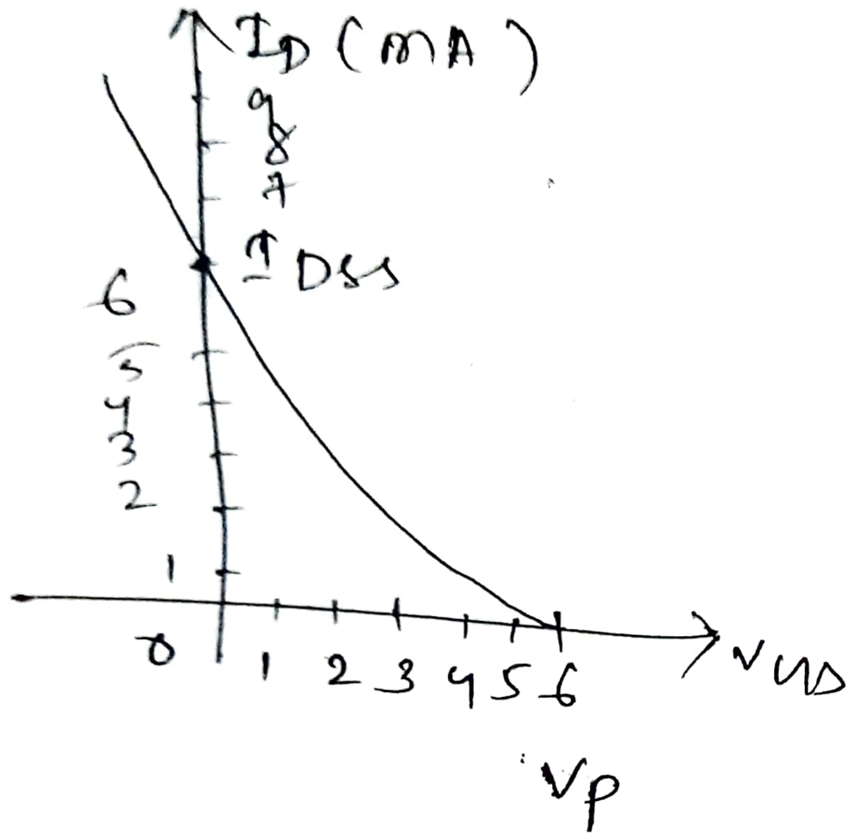


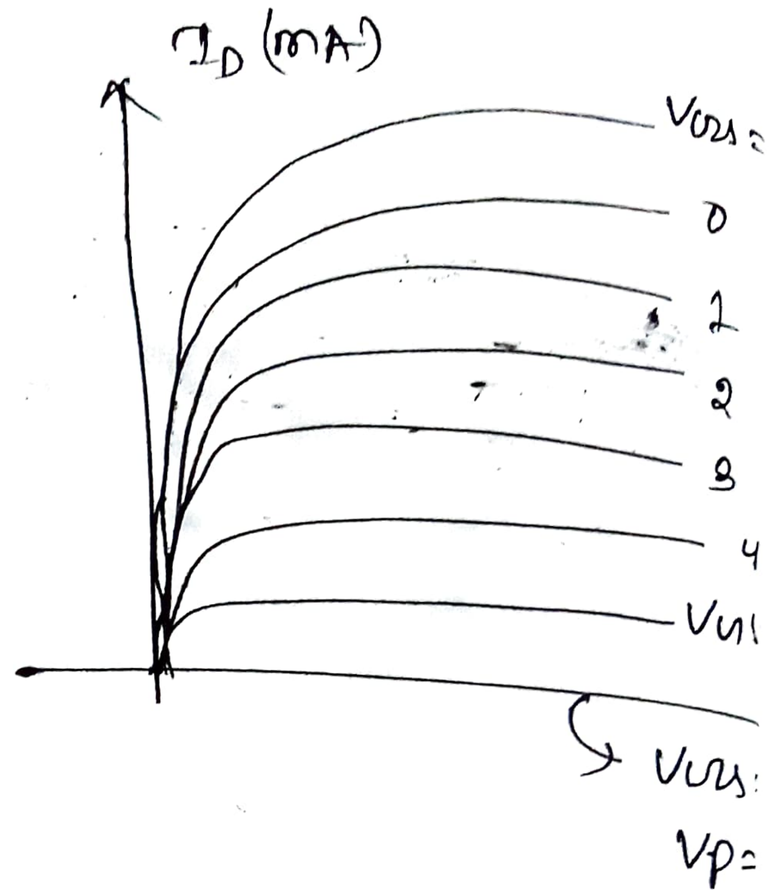
Transfer characteristics

I_D (mA)
I_D (mA)
-6 V
-5V
V_{GS} = -4V
-3V
V_{DS}
V_{GS}
-6 -5 -4 -3 -2 -1
V_T
$V_{GS} = V_T = -2V$

current will increase with -ve values of V_{GS}.

P-channel depletion type mosfet.



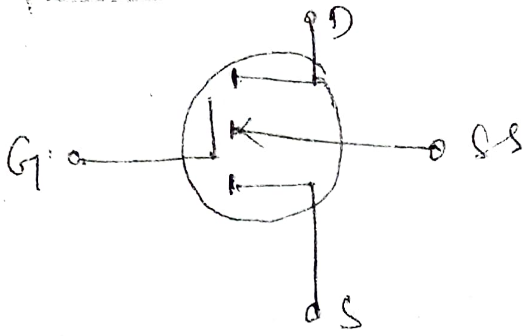


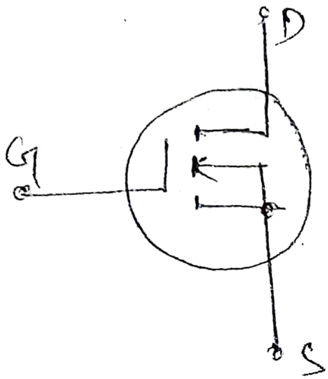
Drain current increase from cutoff at $V_{GS} = V_P$

I_{DS} increase for -values of V_{GS}.

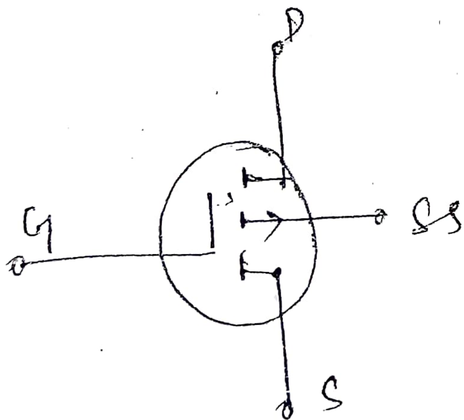
Symbol(s)

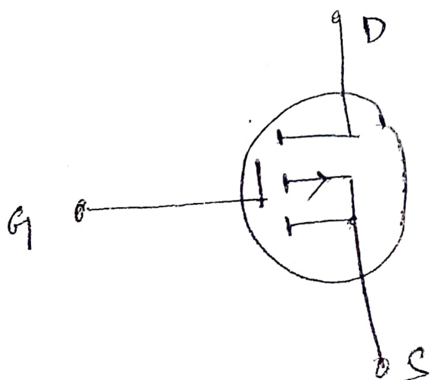
n-channel enhancement type MOSFET





P-channel enhancement type MOSFET





... (fig. 2)

$V_{GS} = 0V$, V_{DS} = some +ve value.

The result is the gate and a source terminal at the same potential & a depletion region in the lower end of each p-type material similar to the no bias condition.

- The instant voltage $V_{DS} = V_{DD}$ is applied, electrons are drawn to the drain terminal establishing current I_D drain terminal.

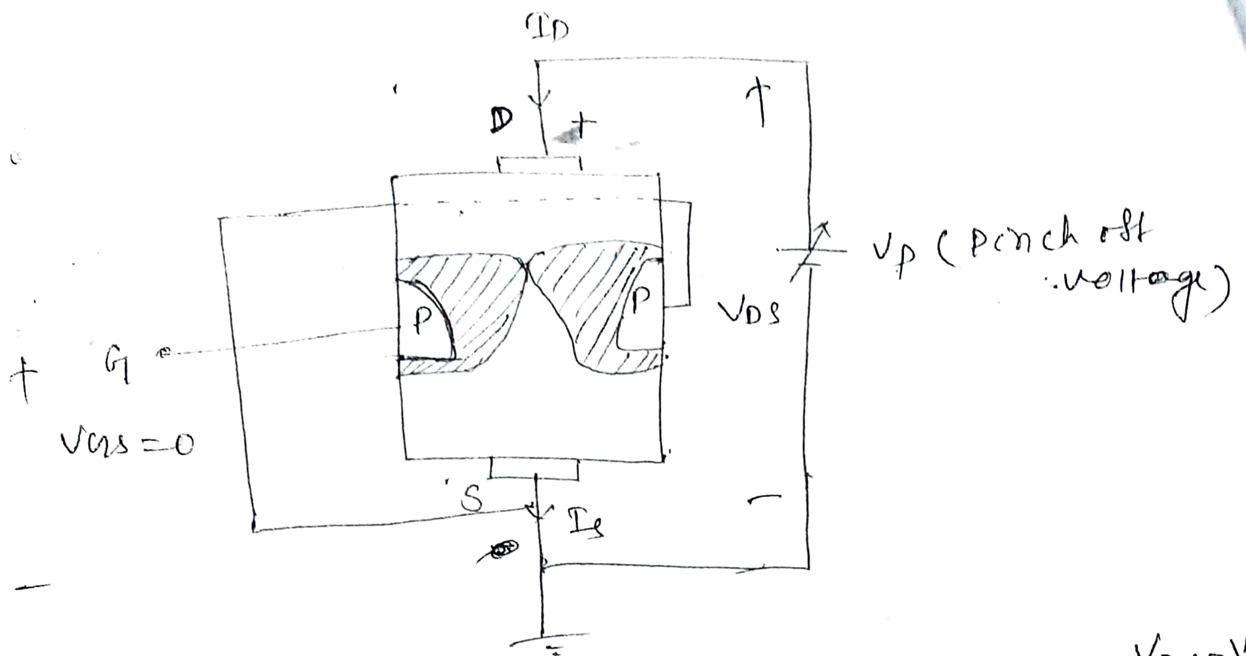
$$I_D = I_S$$

- The region for change in width of the depletion region is due to the fact that different voltage level are set up by the drain current due to non-uniform distribution of resistance in the n-channel.

- Hence the upper region is more reverse biased compared to the lower.

- If V_{DS} is increased from $0 \rightarrow$ few volts current will increase.

N.B. Forward Bias junction has low resistance path & vice versa.



(Fig-2) (pinch off $V_{GS} = 0V$, $V_{DS} = V_p$)

- As V_{DS} increases and approaches the value equal to V_p, then depletion regions will widen causing a reduction in a n-channel.

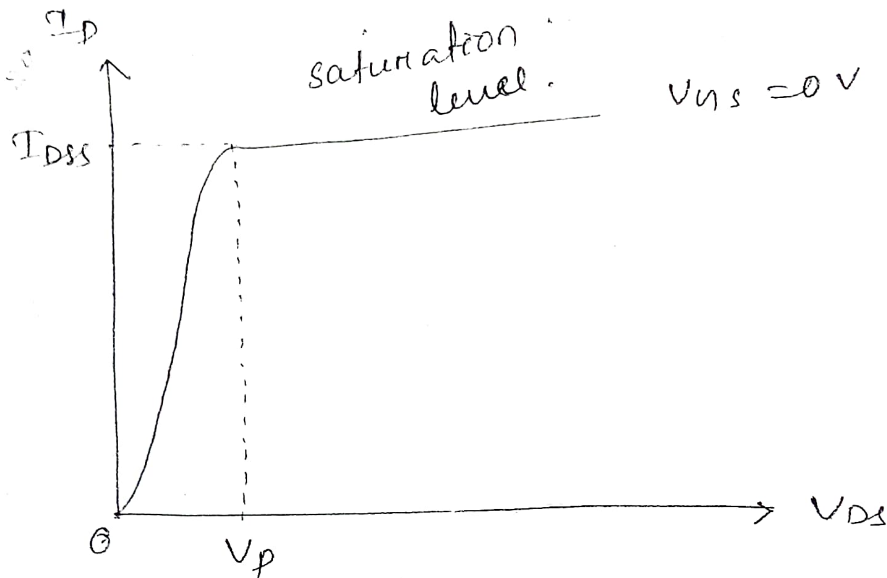
- At this point of time when the two depletion region touch each other, the condition is reffered to as pinch-off. & the voltage is known as pinch off voltage.

- When V_{DS} increases beyond V_p, the region between the depletion region increases in length but I_D remains same and denoted as I_{DSS}.

- I_{DSS} is the maximum current for JFET & is defined by the condition $V_{GS} = 0V$.

$$V_{DS} > |V_p|$$

characteristics.



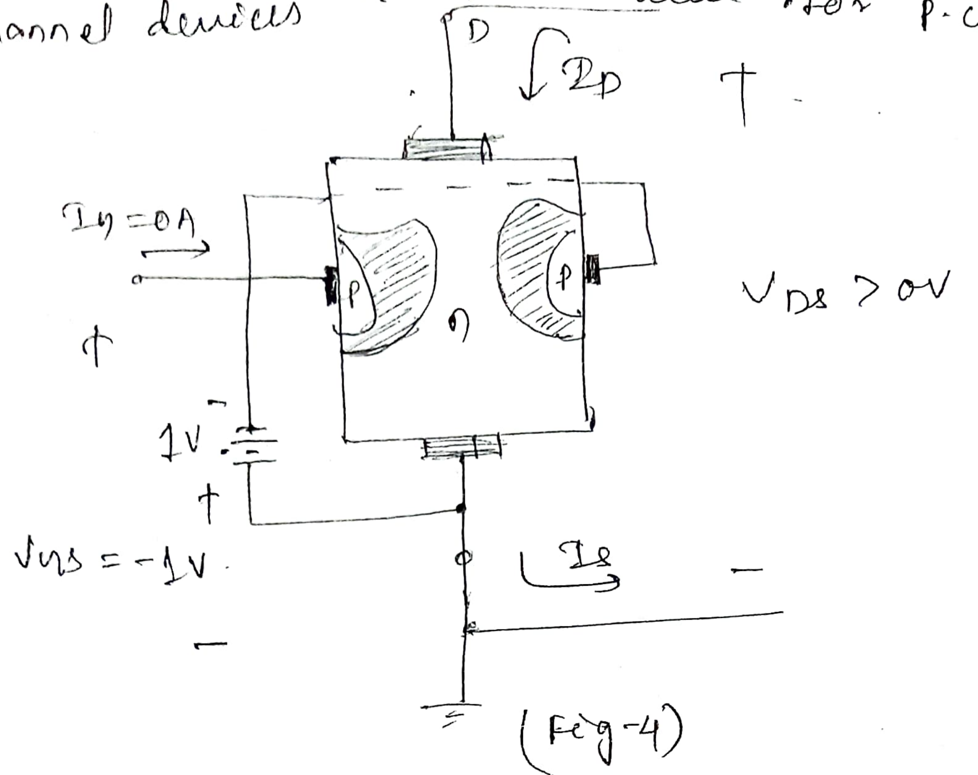
(Fig-3) (I_D vs V_{DS} for $V_{GS} = 0V$)

case-2 (Fig-4)

- A voltage of -1V is applied between gate and source, the current reaches the saturation level earlier as compared to $V_{GS} = 0V$ condition.
- Hence the saturation level will be met at the lower value of V_{DS}.
- when V_{GS} is made more negative i.e equal to $-V_p$. It is sufficiently negative to establish 0mA and the device gets turned off.

Pinch off voltage — It is the minimum drain source voltage at which the drain current essentially becomes constant.

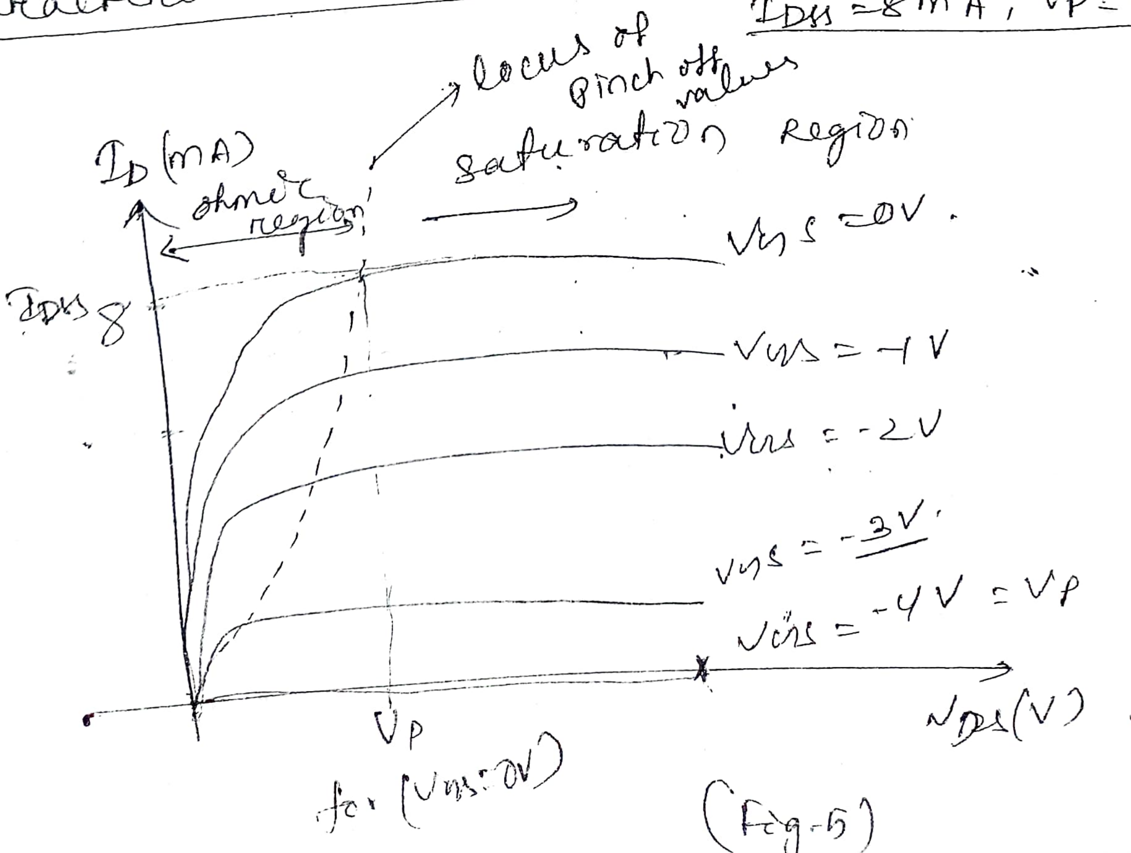
→ The level of V_{GS} that results in $I_D = 0\,mA$ is defined by $V_{GS} = V_P$, with V_P being a -ve voltage for n channel devices & +ve value for p-channel devices.



(Fig-4)

(Application of a negative voltage to the gate of a JFET)

characteristics of n channel JFET with $I_{DSS} = 8\,mA$, $V_P = -4V$.



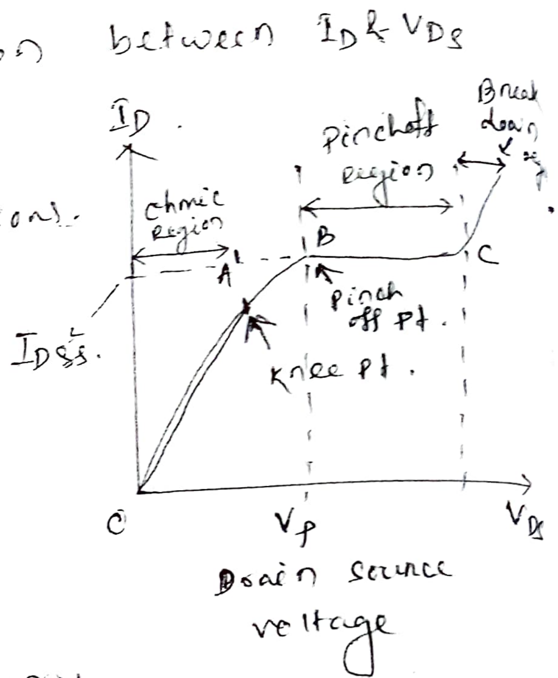
(Fig-5)

Characteristics of a JFET

2 types of characteristics. 1) output / Drain characteristics
2) Transfer characteristics

Drain characteristics :- It gives relation between I_D & V_{DS} for different values of V_{GS}.

- It can be subdivided into 4 regions.



1) Ohmic Region (OA).

- During this period the curve is linear for low values of V_{DS}.

current varies directly with voltage following ohm's law.

i.e JFET behaves like an ordinary resistor till pt. "A" called knee point.

2) Curve (AB) :- I_D increases at a very low rate upto pt B. i.e from pt "A" to pt "B".

- V_{DS} corresponding to pt "B" called pinchoff voltage.

3) Pinch-off Region (BC) :- It is known as saturation or amplified region.

- During this period V_{DS} increases but I_D remains constant & named as I_{DSS}.

- During this period no external bias required as $V_{GS} = 0V$.

~~Drain current region~~

Break down region :- If V_{DS} increases beyond the saturation value, then I_D increases rapidly.

Because the reverse biased gate channel PN junction

? Write the equation for drain current from the [illegible] fig (a) transfer characteristics of a JFET).

Referring to transfer characteristics

$I_{DSS} = 12\,mA.$

$V_{GS(off)} = -5V$

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

$$= 12\left[1 + \frac{V_{GS}}{5}\right]^2 mA$$

A JFET has a drain current of 5 mA. If $I_{DSS} = 10\,mA$ & $V_{GS(off)} = -6V$, find the value of (i) V_{GS} & (ii) V_P.

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

$$5 = 10\left[1 + \frac{V_{GS}}{6}\right]^2.$$

$$1 + \frac{V_{GS}}{6} = \sqrt{\frac{5}{10}} = 0.707$$

$$V_{GS} = (0.707 - 1) \times 6 = -1.76V.$$

$$V_P = -V_{GS(off)} = 6V.$$

MOSFET < D-MOSFET < p-channel; E-MOSFET < n-channel, p-channel. 40

/DE MOSFET. By changing the polarity of V_{GS}, it can operate in both mode.

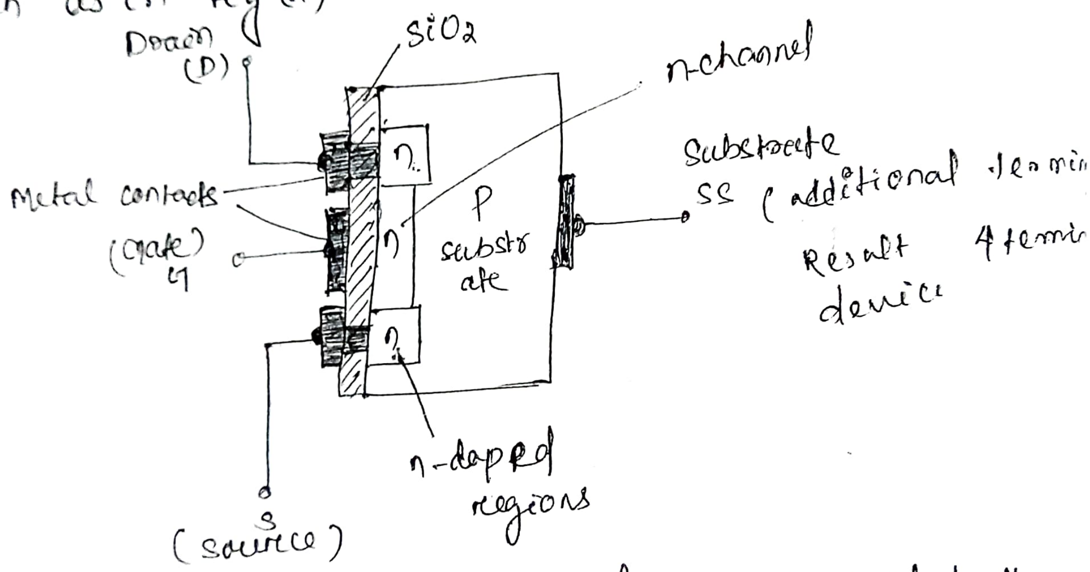
Basic construction

→ A slab of p-type material is formed from a silicon base & is referred to as the substrate

→ It is the foundation on which the device is constructed.

→ The substrate is externally connected to the source terminal.

→ Many discrete device provide an additional terminal labeled SS, resulting in a four-terminal device, such as in fig (a).



→ The source & drain terminals are connected through metallic contacts to n-doped regions linked by an n-channel as shown in fig.

→ The gate is also connected to a metal contact surface but remains insulated from the n-channel by a very thin silicon dioxide (SiO_2) layer.

→ SiO_2 is a type of insulator referred to as a dielectric, which sets up opposing electric fields with dielectric when exposed to an externally applied field.

SiO_2 layer is an insulating layer means that:

- There is no direct electrical connection betwe the gate terminal & the channel of a mosfet
- It is the insulating layer of SiO_2 in the MOSFET construction that accounts for the very desirable high i/p impedance of the device.

so $I_G = 0$

- The input resistance of a MOSFET is more than that of a typical JFET, even though the input impedance of most JFETs is sufficiently high for most applications.

- B'coz of high i/p impedance $I_G = 0A$ for dc bias configuration.

- In MOSFET
  - Metal for drain, source & gate
  - oxide for silicon dioxide insulating layer.
  - semiconductor for the basic structure on which the n- and p-type regions are diffused.

- The insulating layer between the gate and the channel has resulted in another name for the device: insulated-gate FET, or IGFET.

BASIC OPERATION AND CHARACTERISTICS

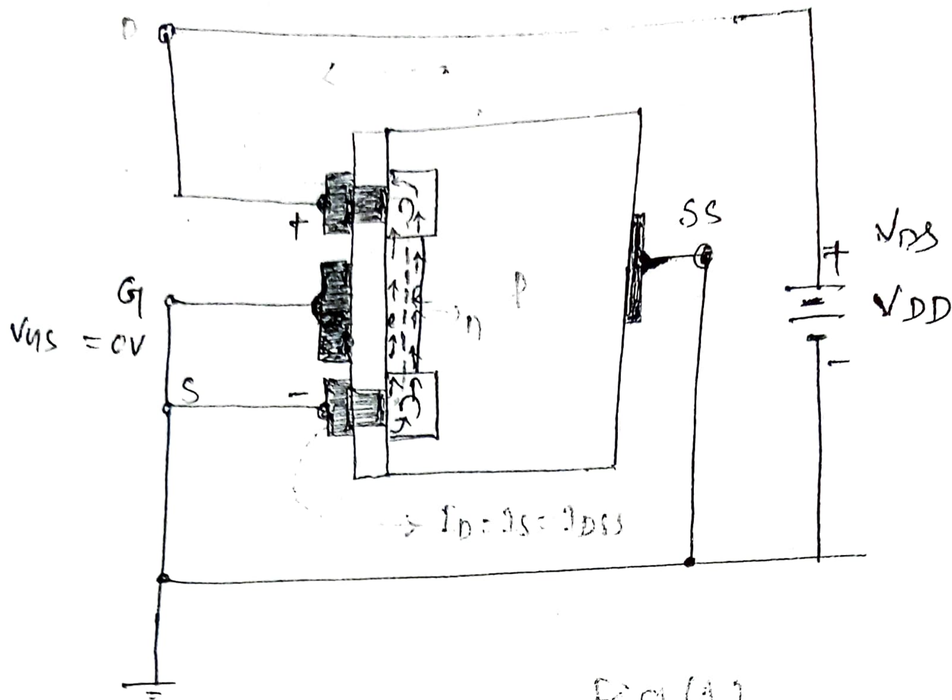


Fig (1)

~~n-type~~ n-channel depletion-type MOSFET with $V_{GS} = 0V$ & applied voltage V_{DD}.

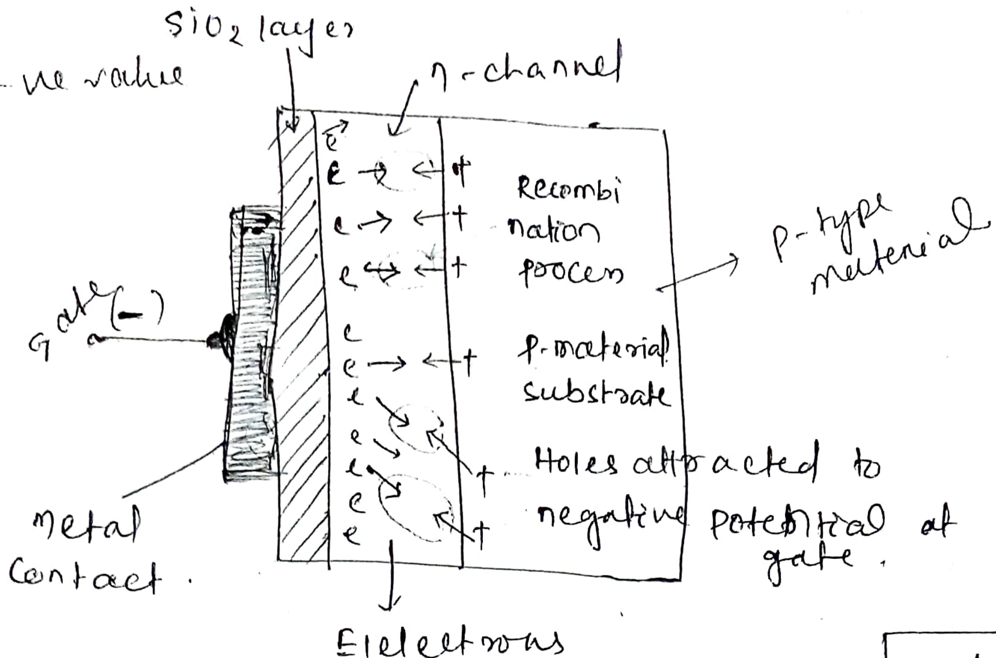
Case - I $V_{GS} = 0V$, V_{DS} = +ve value

→ The gate & source voltage is set to 0V by the direct connection from one terminal to the other & a voltage V_{DS} is applied across the drain-to-source terminals.

→ The result is an attraction for the positive potential at the drain by the free electrons of the n-channel and a current similar to that established through the channel of the JFET.

Case - II

V_{GS} = -ve value



(fig-3)

$V_{GS} \uparrow$ $I_D \downarrow$

Reduction in free ~~Electrons~~ carriers in a channel due to a negative potential at the gate terminal.

→ V_{GS} is set at negative voltage such as -1V.

→ The -ve potential at the gate will tend to pressure electrons toward P-type substrate (like charges repel) & ~~holes~~ attracts holes from the p-type substrate (opposite charges attract) as shown in the above figure.

→ Depending on the magnitude of the negative bias established by V_{GS}, a level of recombination between electrons & holes will occur that will reduce the number of free electrons in the n-channel available for conduction.

→ The more negative the bias, the higher is the rate of recombination.

→ The resulting level of drain current is therefore reduced with increasing negative bias for V_{GS}.

Case - III V_{GS} : +ve value, the +ve gate will draw the addition electrons (minority carriers) from p-type material.

→ If we apply $V_{GS} = 4V$ then $I_D = 22.2 mA$.

→ If V_{GS} increase I_D increase at a maximum rapid rate.

That means I_D exceed the rating (current or power) for the device.

[$V_{GS} \uparrow I_D \uparrow$]

→ The application of a positive gate-to-source voltage has "enhanced" the level of free carriers in the channel compared to that encountered with $V_{GS} = 0V$.

→ So region of positive gate voltages on the drain / transfer characteristics is often reffered to as the enhancement region.

→ The region bet^n cutoff & saturation level of I_{DSS} referred to as the depletion region.

→ The relationship bet^n I_D & V_{GS} is defined by shockley's equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Control variable: V_{GS}

Constants: I_{DSS}, V_P

$$I_D = \begin{cases} I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 & V_{GS} > V_P \text{ (n-channel)} \\ & V_{GS} < V_P \text{ (p-channel)} \\ 0 & \text{otherwise} \end{cases}$$

Transfer characteristics :-

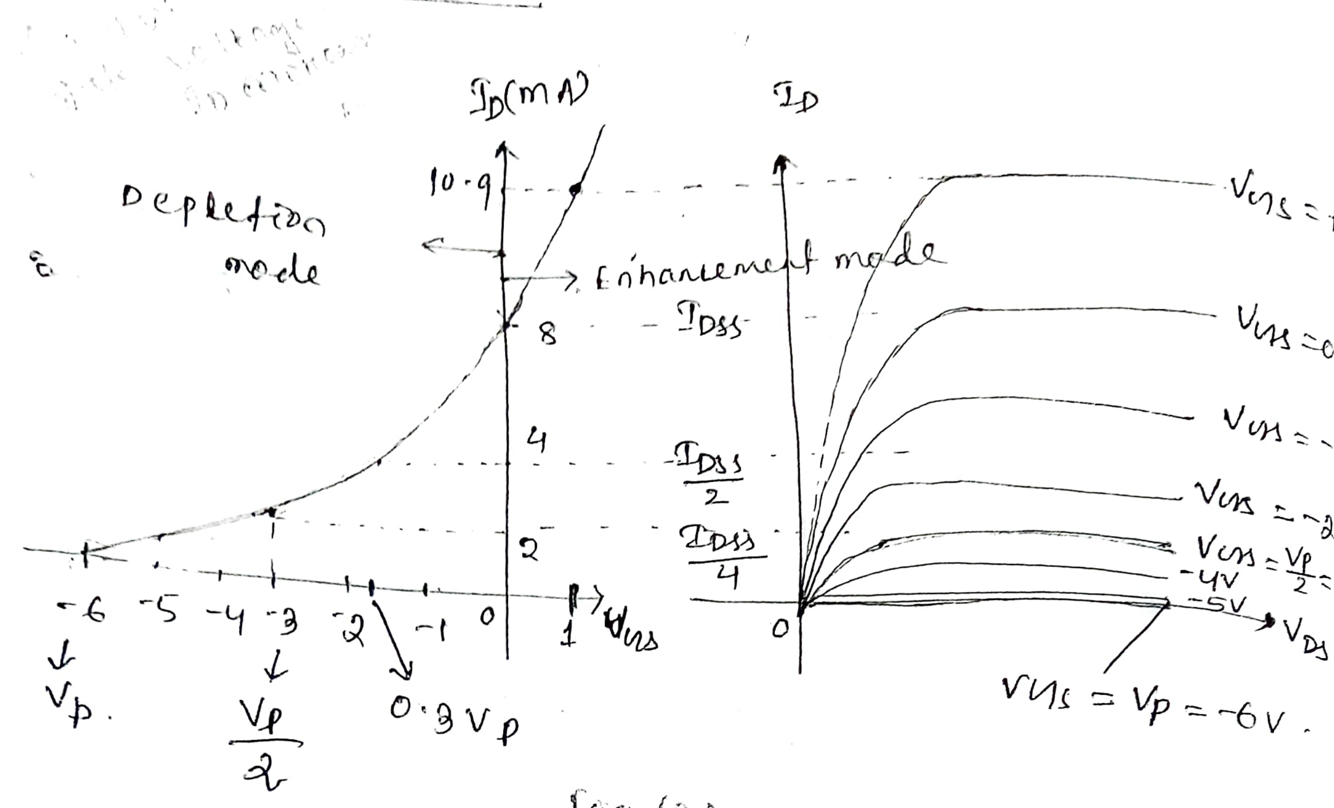


Fig (2)

Drain characteristic & Transfer characteristics for an n-channel Depletion mode MOSFET.

From above figure :-

i) I_{DSS} (shorted-gate drain current) :- It is the drain current with source short-circuited to gate (i.e $V_{GS} = 0$) and drain voltage (V_{DS}) equal to pinch off voltage. It is sometimes called zero-bias current.

ii) V_{DS} - ~~Maximum~~ drain to source voltage

iii) V_{GS} - Gate to source voltage

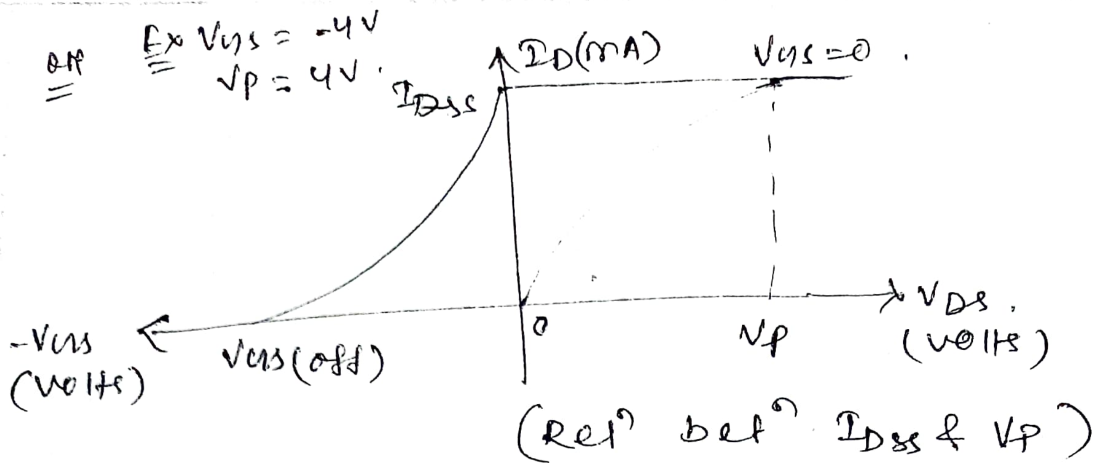
iv) I_D - drain current

v) V_P (pinch off voltage) - It is the minimum drain-source voltage at which the drain current essentially becomes constant.

If $V_{DS} > V_P$ → then JFET can operate.

If $V_{DS} > V_{DS(max)}$ → then JFET breakdown.

or Ex $V_{GS} = -4V$
$V_P = 4V$



(Rel^n bet^n I_{DSS} & V_P)

Expression for drain current I_D :-

$V_{GS(off)}$ → Gate-source cut off voltage : It is the gate-source voltage where the channel is completely cut off and the drain current becomes zero.

$V_P = V_{GS(off)}$ (∵ By drain characteristic)

so $$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

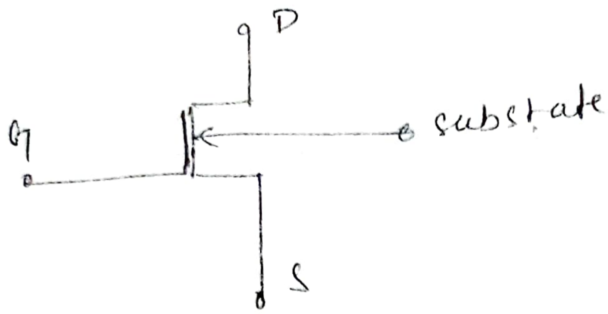
I_D = drain current at given V_{GS}.

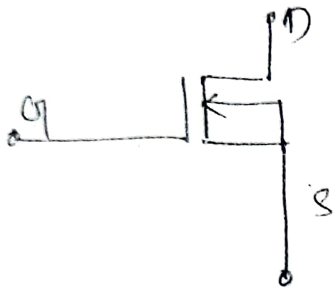
I_{DSS} = Shorted - gate drain current

V_{GS} = gate- source voltage.

$V_{GS(off)}$ = gate - source cut off voltage.

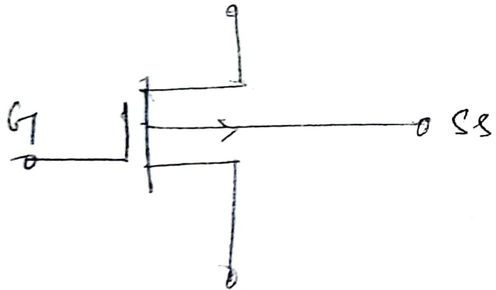
symbol

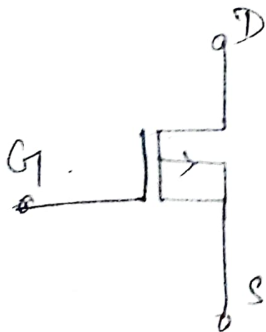




substrate connected to source

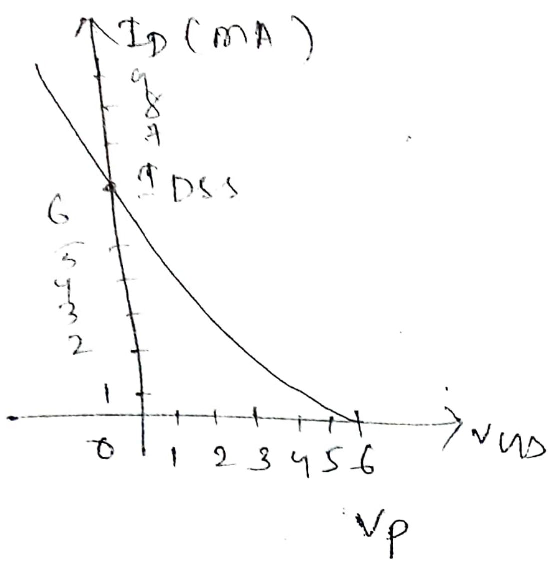
(n-channel depletion-type mosfet)

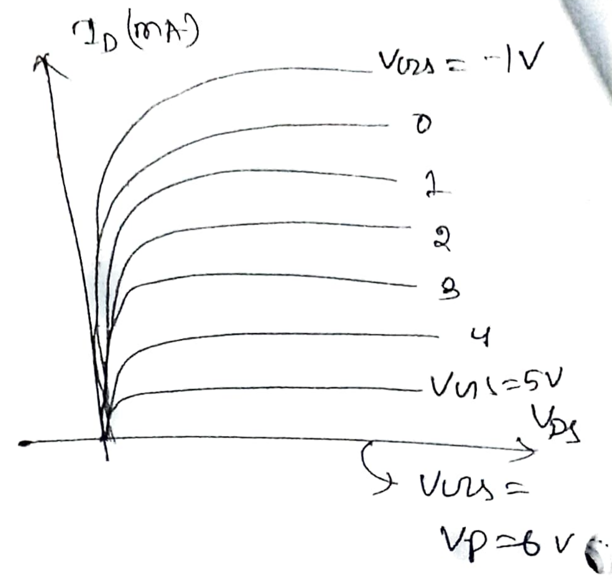




(p-channel depletion-type Mosfet)

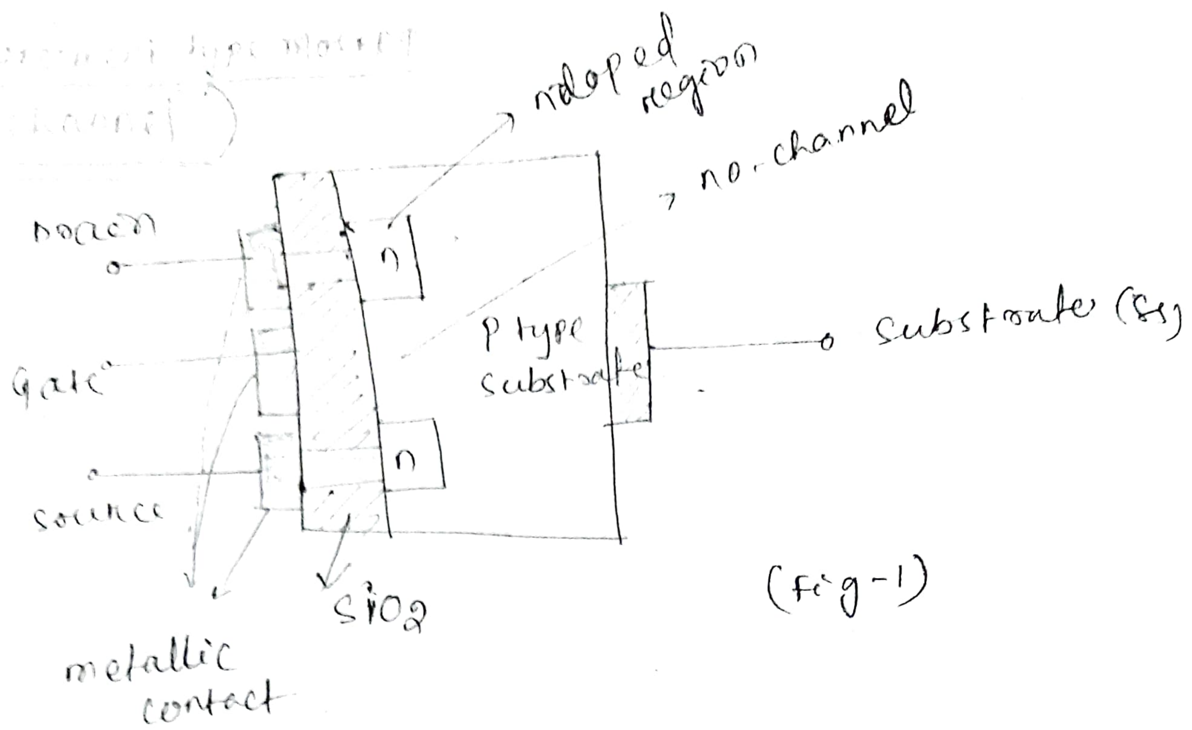
p-channel depletion type mosfet





Drain current increase from cutoff at $V_{GS} = V_P$.

I_{DS} increase for -values of V_{GS}.



(n-channel enhancement type MOSFET)

→ A slab of p-type material is taken & is treated as substrate.

→ The source & drain terminals are connected to n-dopped regions but no-channel is present between the two n-dopped regions. This is the primary difference between the construction of depletion type & enhancement type MOSFET.

→ The SiO_2 layer is present to isolate the region between drain & source from the gate.

Case-I

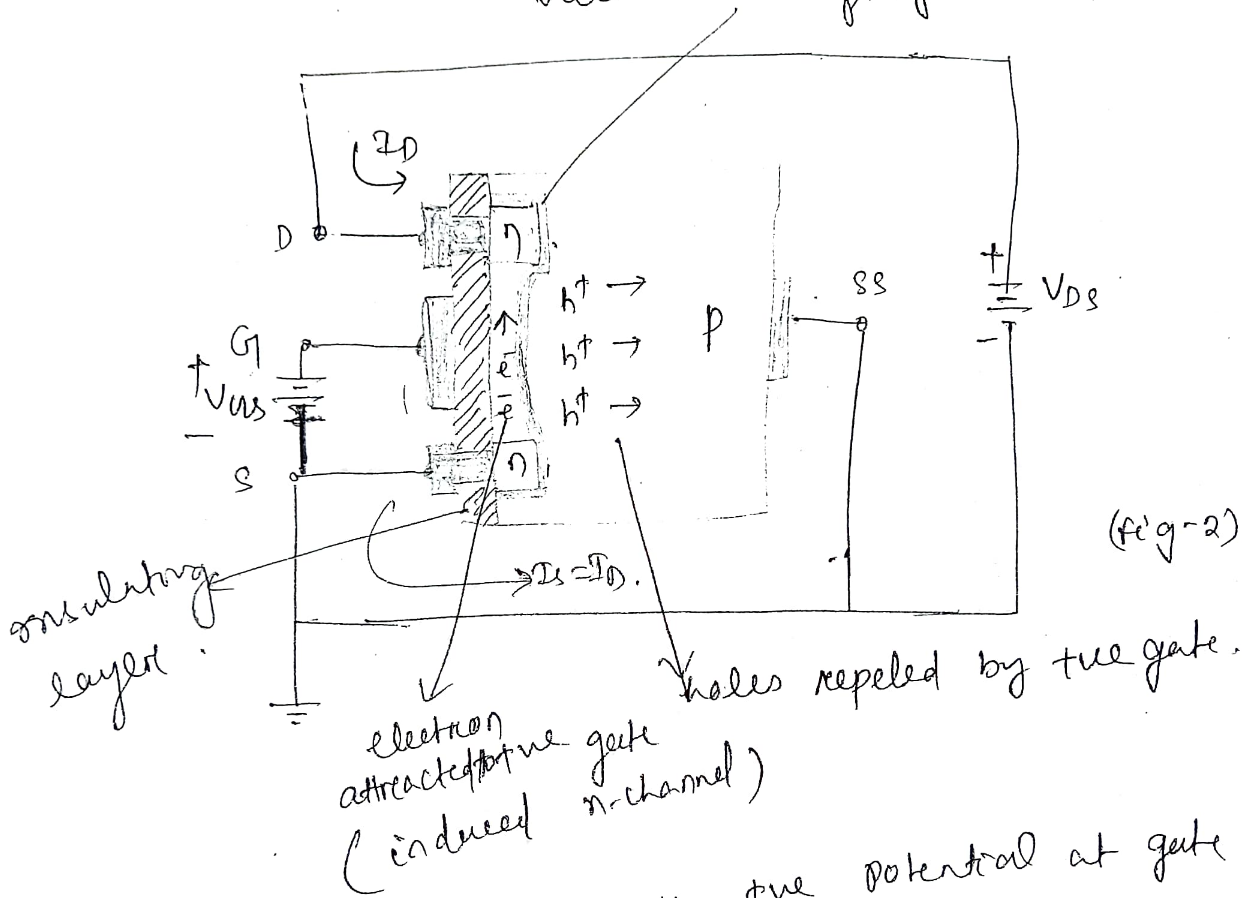
$V_{GS} = 0\,V$, V_{DS} = +ve value

The absence of n-channel will result in a current of 0A because it is not sufficient to have a large accumulation of carriers (electrons) at the drain & source if a path

fails to exist between the two.

- In fact the two reverse biased p-n junction between n-dopped region & p-type substrate opposes the flow of electron between drain & source.

Case - II $V_{GS} = V_{DS}$ = some +ve value.



- When V_{GS} = +ve value, the +ve potential at gate will pressure the holes along edge of the SiO_2 layer to enter the dipper into p-type material. The result is depletion layer near to the SiO_2 layer void of holes.

- The electrons in the p-type subscript will be attracted to the gate & accumulate in the region nearer to SiO_2 layer.

- As V_{GS} increases, concentration of e^- increases until the induced n-type layer supports a measureable flow of current between the drain and the source.

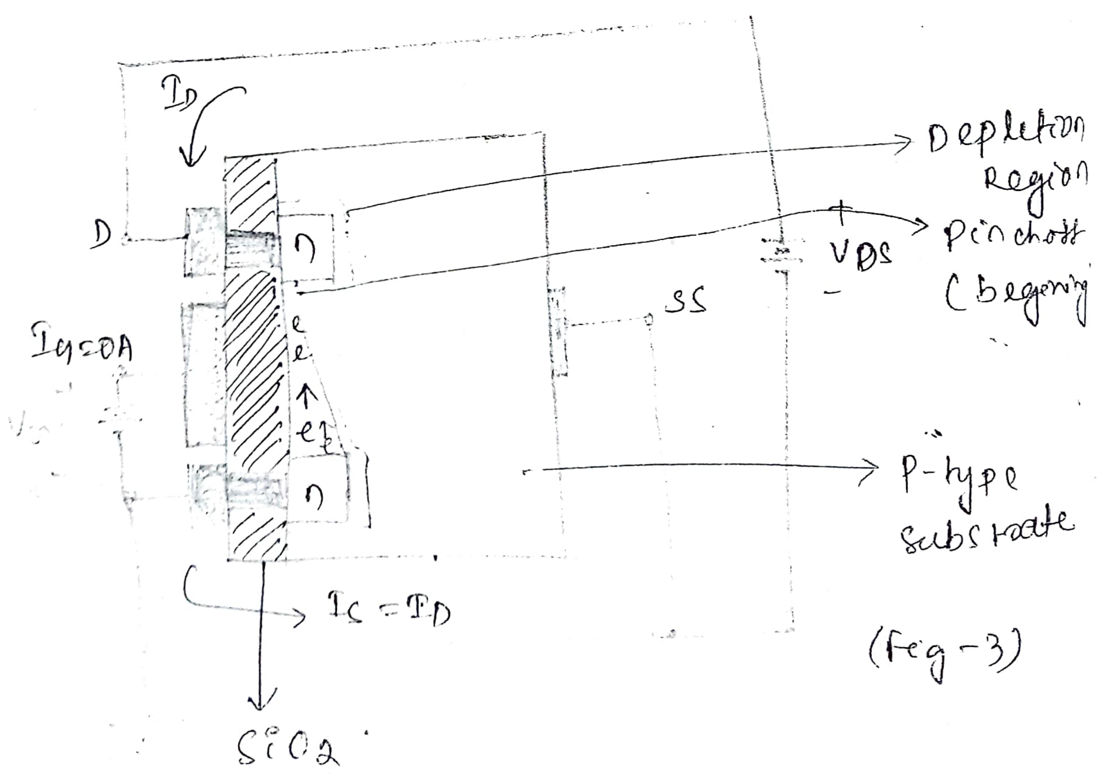
Threeshold voltage :-

The level of V_{GS} that results in significant increase in the drain current is called threshold voltage given by V_T.

- Since the channel is absent with $V_{GS} = 0V$, and is enhanced by the application of +ve V_{GS}. This type of MOSFET is known as enhancement type MOSFET.

Case - III

V_{GS} = constant, V_{DS} = +ve value.

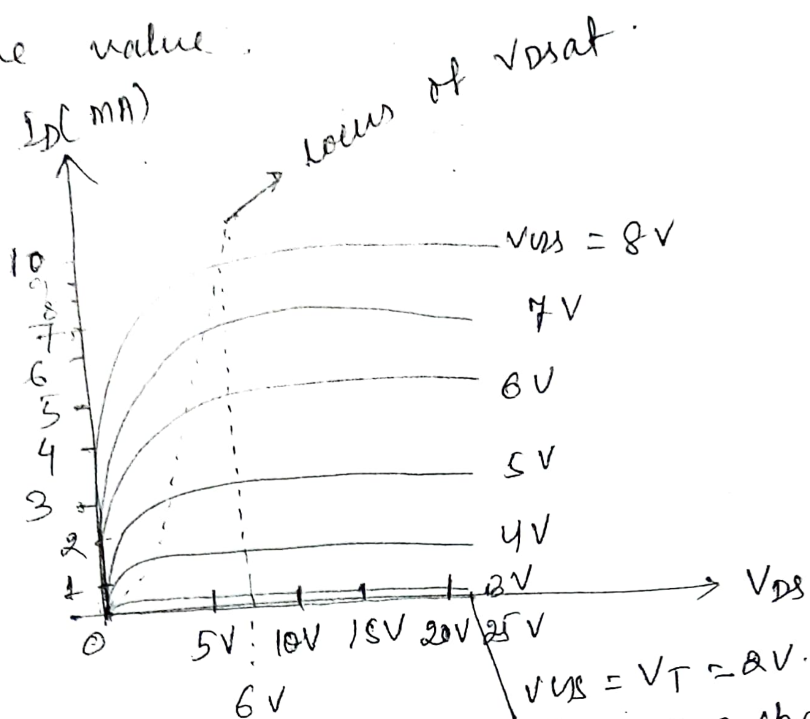


(Fig-3)

(change in channel and depletion region with increasing level of V_{DS} for a

V_{GS} = constant

V_{DS} = +ve value.



(Drain characteristics of an n-channel enhancement-type MOSFET with $V_T = 2V$ & $K = 0.278 \times 10^{-3}\ A/V^2$)

- If we increase the value of V_{DS} & V_{GS} = const the drain current reaches the saturation value. This is due to the pinch off process that occurs by narrowing a channel at the drain end of the MOSFET.

$$V_{DG} = V_{DS} - V_{GS}$$

$$(V_{DS})_{sat} = V_{GS} - V_T$$

for $V_{GS} < V_T$, $I_D = 0\,mA$

For $V_{GS} > V_T$, $I_D = K(V_{GS} - V_T)^2$

- where K is a constant and is a function of construction of the device and is defined by K.

$$K = \frac{I_{D}(on)}{\{V_{GS}(on) - V_T\}^2}$$

- Here $I_D(on)$ and $V_{GS}(on)$ are the values at a particular operating point on the MOSFET characteristics.

Let $I_D(on) = 10 mA$
$V_{GS}(on) = 8 V$ } from fig-4
$V_T = 2V$.

$$K = \frac{10 mA}{(8V - 2V)^2}$$

$$= \frac{10 mA}{(6V)^2}$$

$$= \frac{10 mA}{36 V^2} = 0.278 \times 10^{-3} A/V^2.$$

$$I_D = K(V_{GS} - V_T)^2$$

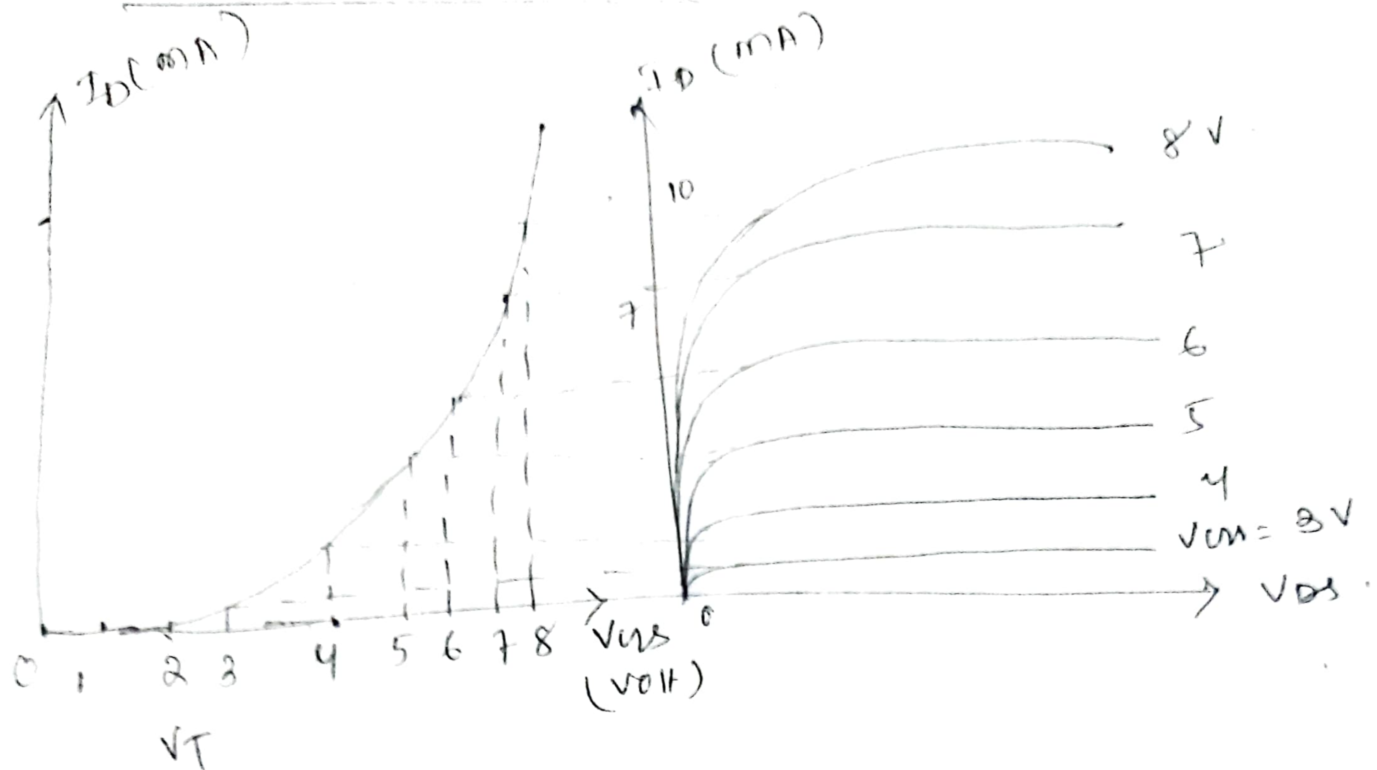
$$= 0.278 \times 10^{-3} (V_{GS} - 2V)^2.$$

substituting $V_{GS} = 4V$.

$$I_D = 1.11 mA$$

At $V_{GS} = V_T$ $I_D = 0 mA$.

Transfer characteristics



$I_B = 80 \mu A \quad V_{CE} = 5V$

$\beta_{ac} = ?$

$$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B}\Big|_{V_{CE}=const.} = \frac{I_{C2} - I_{C1}}{I_{B2} - I_{B1}}.$$

$I_C = 6.7 \, mA$

Transistor Biasing.

Basically a transistor is used as an amplifier. The process of raising the strength of a weak signal without any change in its general shape is referred to as *faithful amplification*. (*)

The basic requirement for faithful amplification are (CE)

(i) emitter-base junction is forward biased.

(ii) Collector-~~base~~ emitter junction is reverse biased.

(iii) Proper zero signal collector current.

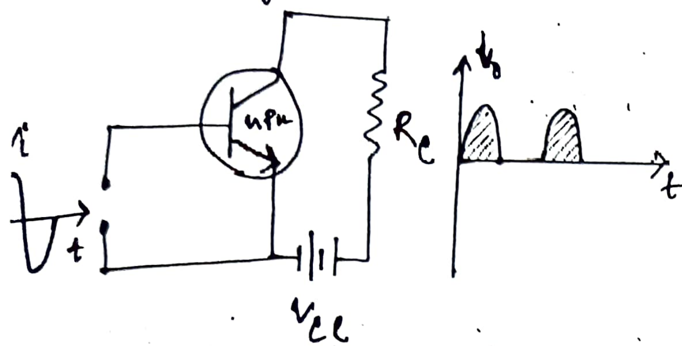
~~(i) Emitter-base junction~~

(i) **Minimum proper base-emitter voltage:** The base emitter voltage V_{BE} should not fall below 0.3V for germanium & 0.7V for silicon transistor at any instant. If V_{BE} falls below these values during any part of the signal, that part will be amplified to smaller extent due to smaller collector current & therefore faithful amplification can not be accomplished.

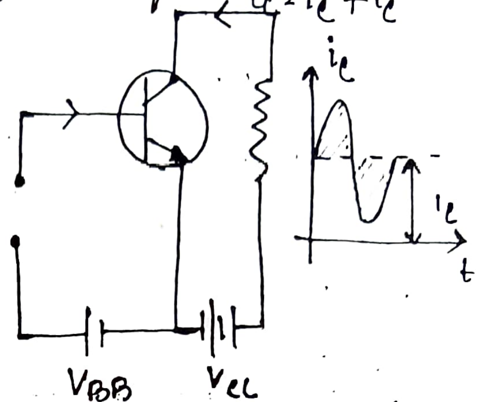
(ii) **Minimum proper collector-emitter voltage:** There must be a proper reverse bias voltage across collector to emitter voltage V_{CE} which value is 0.5V ~~for~~ Ge and 1V for Si transistor. If V_{CE} falls below these values the collector-emitter junction is not properly reverse bias causing increase in base current I_B and decrease in collector current I_C & so decrease in the value of β & result in unfaithful amplification.

(iii) **Proper zero signal collector current:** Consider an npn transistor ckt. as shown in fig (i). During the positive half-cycle of the signal base is positive w.r.t. emitter and hence base-emitter junction is forward

biased. This will cause a base current and much larger collector current to flow in the circuit. The result is that +ve half-cycle of the signal is amplified in the collector as shown. However, during the -ve half-cycle of the signal base-emitter junction is reverse biased and hence no current flows in the circuit. The result is that there is no output due to the negative half-cycle of the signal. So we get unfaithful amplification.



Unfaithful Amplification



Faithful Amplification

Now, introduce a battery source V_{BB} in the base ckt. The magnitude of this voltage should be such that it keeps the i/p circuit forward biased even during the peak of -ve half-cycle of the signal. When no signal is applied a d.c. current I_C will flow in the collector circuit due to V_{BB}. This is known as zero signal collector current I_C. During the positive half-cycle of the signal, i/p ckt is more forward and hence collector current increase. However, during the -ve half cycle of the signal, the i/p ckt is less forward biased and collector current decreases. In this way the -ve half cycle of the signal also appears in the o/p and hence faithful amplification results. So, for faithful amplification zero signal collector current must be flow.

∴ Zero signal collector current ≥ max. collector current due to signal alone.

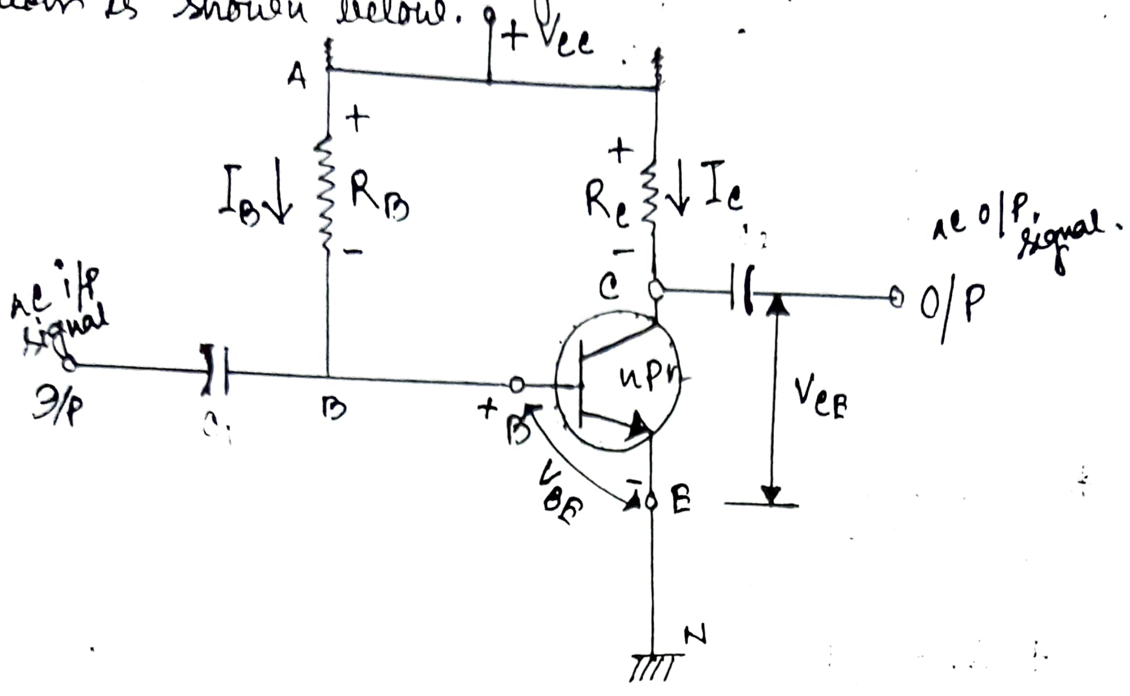
Four types of biasing ckt are there:

1. Fixed bias
2. Emitter stabilized bias
3. Voltage divider bias
4. DC-bias with voltage feed back.

The proper flow of zero signal I_C and the maintanance of proper collector-emitter voltage during the passage of signal is called the transistor biasing.

1. FIXED-BIAS CIRCUIT:

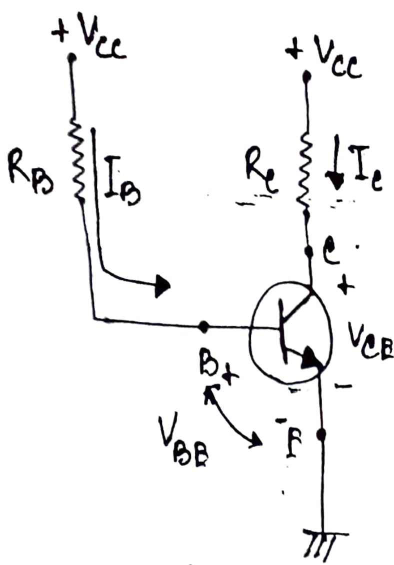
* The circuit arrangement of a fixed-bias configuration is shown below.



* In this method, a high resistance R_B (several hundred KΩ) is connected between the base and +ve end of supply for npn transistor and between base and negative end of supply for pnp transistor. Here the required zero signal base current is provided by V_{cc} and it flows through R_B. It is because now base is positive w.r.to emitter i.e. base-emitter junction is forward biased. The required value of zero signal base current I_B (and hence $I_C = \beta I_B$) can be made to flow by selecting the proper value of base resistor R_B.

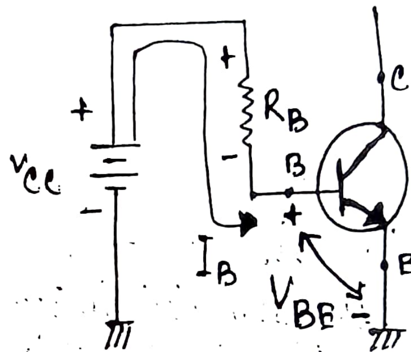
* Circuit analysis: It is required to find the value of R_B so that required collector current flows in the zero signal conditions. Let I_C be the required zero signal collector current.

$$\therefore I_B = \frac{I_C}{\beta}$$



DC equivalent circuit.

* First Applying KVL to calculate the base-emitter loop:

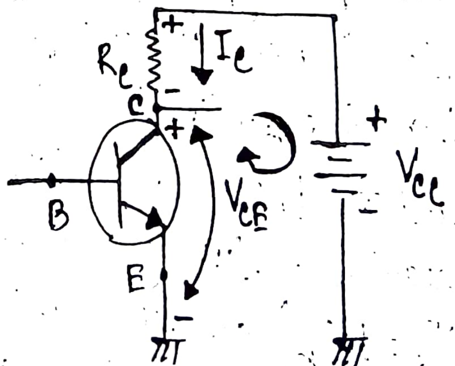


Base-emitter loop.

$$+V_{cc} - I_B R_B - V_{BE} = 0$$

$$\Rightarrow \boxed{I_B = \frac{V_{cc} - V_{BE}}{R_B}}$$

* Now applying KVL to the collector-Emitter loop:



~~$V_{cc} - I_c R_c - V_{CE} = 0$~~

$$-V_{cc} + V_{CE} + I_c R_c = 0$$

or, $\boxed{V_{CE} = V_{cc} - I_c R_c}$

Again according to single & double subscript notations we have

$\longrightarrow$ $\boxed{V_{CE} = V_c - V_E} \Rightarrow \boxed{V_{CE} = V_c}$ $[\because V_E = 0]$

$\longrightarrow$ $\boxed{V_{BE} = V_B - V_E} \Rightarrow \boxed{V_{BE} = V_B}$ $[\because V_E = 0]$

Advantage: 1) The circuit is quite simple.

Disadvantage: 1) As we are getting a fixed value of I_B, when temparature changes I_{CO} varies & correspondingly I_C changes thereby changing the position of Q-point. Thus the circuit is not stable.

Load line:

~~We have $V_{CE} = V_{CC} - I_C R_C$~~

~~Hence when $V_{CE} = 0V$, $I_C = V_{CC}/R_C = I_C(max)$~~

Purpose of BJT Biasing:

Transistors are used in different kinds of circuits that are designed to serve different purposes. In case of transistors amplifier, we need to use the active region of the transistor output characteristic. The transistor parameters are not absolute constant, but changes with both temparature and bias conditions. For example, transistors β increase with temparature as well as with collector current and an increase of β in turn further increase in collector current. The bias point thus shifts with temparature. Another parameter that affects the bias point is the collector-to base leakage current which approximately doubles for every $10^{\circ}C$ rise in temperature. It may be mentioned that the linear relationship between I_C and I_B ($\Delta I_C = \beta \Delta I_B$) holds true for some particular ranges of I_C and V_{CB}.

The purpose of dc biasing of a transistor is to obtain the most appropriate values of I_C, I_B and V_{CB}. The particular set of values (dc) of I_C,

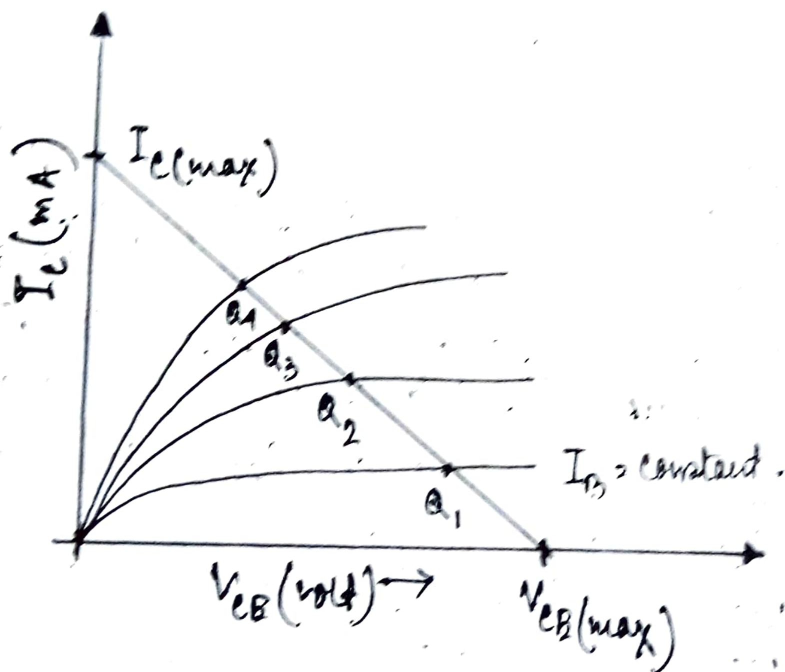
I_B and V_{CE} represents a particular point in the o/p characteristics of the transistor, called the Q point or operating point. To obtain a suitable operating point we make use of some circuit and these ckt are called biasing circuit.

Load line:

We have $V_{CE} = V_{CC} - I_C R_C$

Hence when $V_{CB} = 0V$; $I_C = V_{CC}/R_C = I_{C(max)}$

when $I_C = 0mA$ $V_{CB} = V_{CC} = V_{CB(max)}$



Bias Stability:

* In case of fixed bias circuit $I_B = \frac{V_{CC} - V_{BB}}{R_B}$ i.e. a fixed / constant value & we have

$I_C = \beta I_B + (\beta+1) I_{CBO}$. As the transistors are semiconductor device due to change in temp. I_{CO} changes so β value also changes.

* Hence whenever there is change in temp or change in transistors parameters I_C changes thereby shifting the position of Q-point.

2. EMITTER-STABILIZED BIAS:

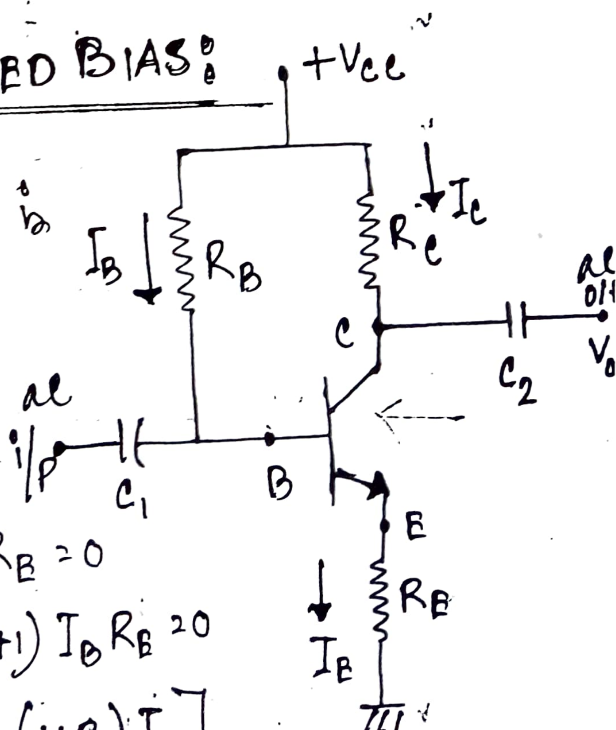
* Therefore we can conclude that maintaining I_B constant will not provide operating-point stability as β changes. On the contrary I_B should be allowed to change so as to maintain I_C & V_{CE} const. irrespective of any change.

* Such condition can be accomplished by using a resistance across R_E. i.e. whenever I_C changes there will be equal change in I_E & that change will change the value of I_B thereby keeping the value of I_C & V_{CE} constant & Q-point constant because if there will be R_E, then we have

$$I_B = \frac{V_{CC} - V_{BE} - I_E R_E}{R_B}$$

2. EMITTER-STABILIZED BIAS:

The ckt arrangement of Emitter-stabilized Bias ckt is like that.



* First applying KVL to the base-emitter loop:

$$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

or, $V_{CC} - I_B R_B - V_{BE} - (\beta+1) I_B R_E = 0$

$$\left[\because I_E = (1+\beta) I_B\right]$$

$$\Rightarrow \boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta+1) R_E}}$$

* Again we have $I_C = \beta I_B$

* Now applying KVL to the collector - emitter loop we have.

$$-V_{CC} + I_B R_B + V_{CB} + I_C R_C = 0.$$

$$\Rightarrow -V_{CC} + I_C R_B + V_{CB} + I_C R_C = 0 \quad [\because I_B \simeq I_C]$$

$$\Rightarrow V_{CB} = V_{CC} - I_C(R_C + R_B)$$

* Again according to single & double subscript notation we have

$$\rightarrow V_{CB} = V_C - V_B$$

$$\text{or, } V_C = V_{CB} + V_B$$

$$\text{or, } V_C = V_{CC} - I_C(R_C + R_B) + V_B$$

$$= V_{CC} - I_C R_C - I_C R_B + V_B$$

$$\rightarrow V_C = V_{CC} - I_C R_C \quad [\because I_C R_B = V_B]$$

$$\rightarrow V_{BB} = V_B - V_B.$$

$$\text{or, } V_B = V_{BE} + V_B$$

$$\text{or, } V_B = V_{CC} - I_B R_B$$

Load line :

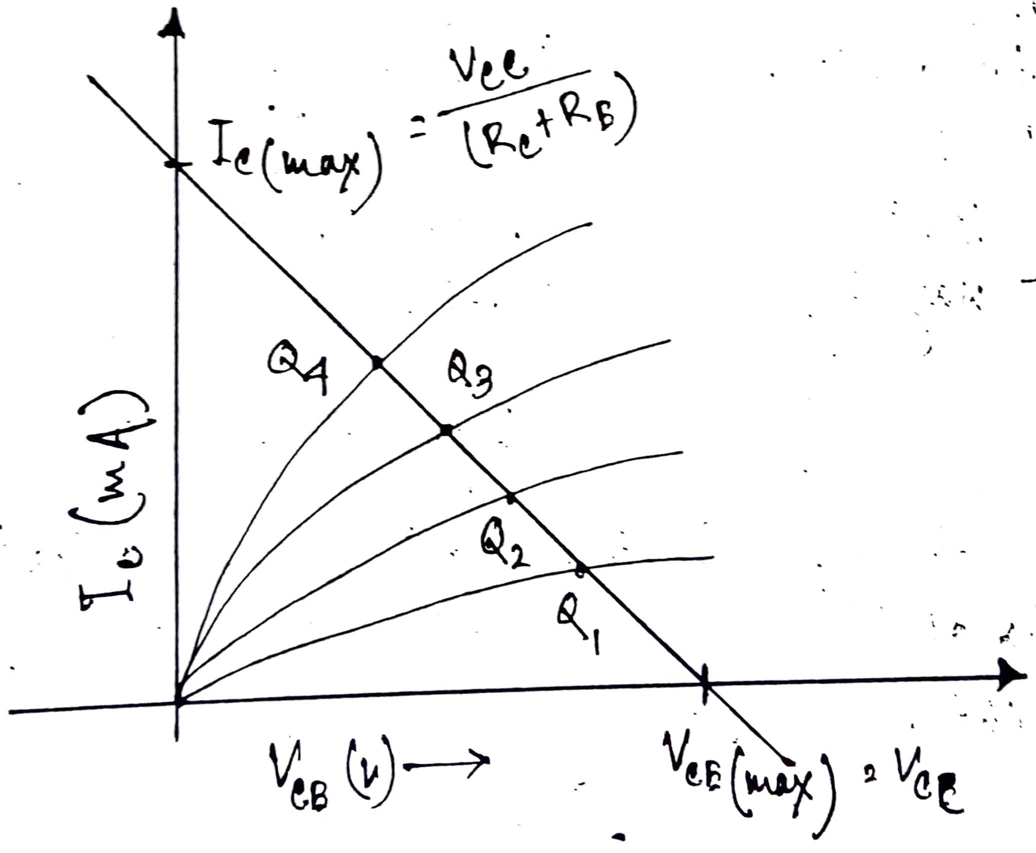
We have $V_{CB} = V_{CC} - I_C(R_C + R_B)$

Hence when $V_{CB} = 0V$; $I_C = V_{CC}/(R_C + R_E)$

$= I_C(max)$

when $I_C = 0mA$;

$V_{CE} = V_{CC} = V_{CE}(max)$



Voltage Divider Bias:

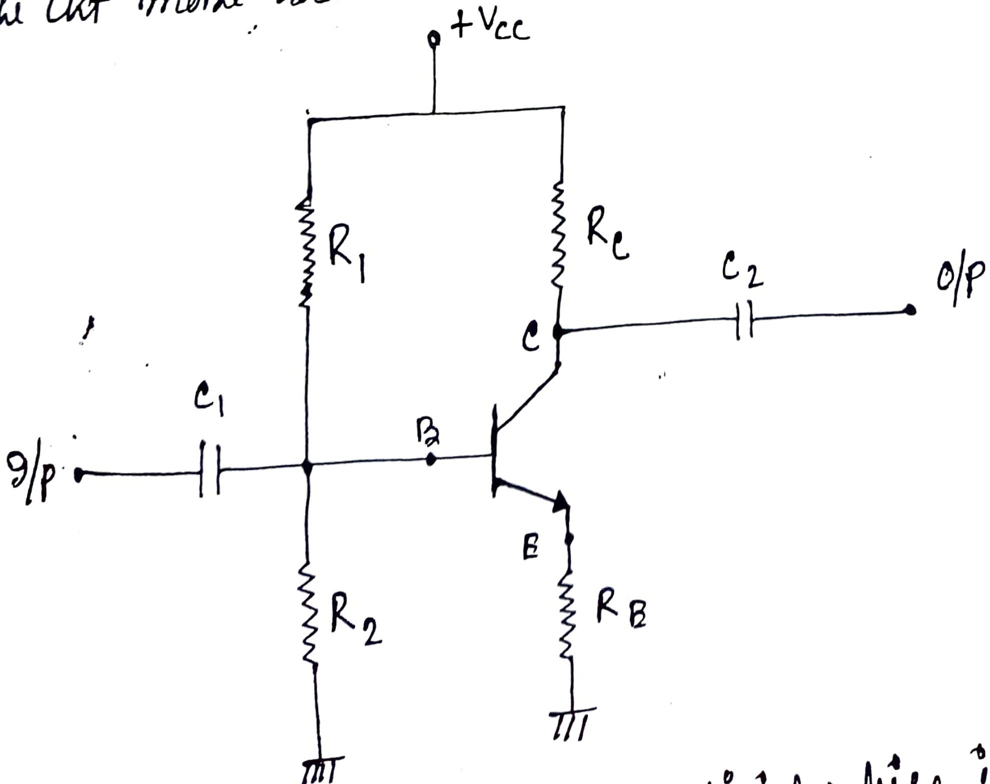
In case of emitter stabilized bias the presence of R_E allows I_B to change so that Q-point will be stable irrespective of variation of temp. But I_C is dependent upon β also. Hence in the emitter-stabilized bias network V_{CE} & I_C were a function of β of the transistor & the actual value of β is usually not well defined.

Hence it would be desirable to develop a bias circuit i.e. less dependent upon β or independent of β. The voltage divider network is such a network which will fullfill such requirements.

Basically we can analyze the network in two different ways; i.e. ① Exact Analysis

② Approximate Analysis.

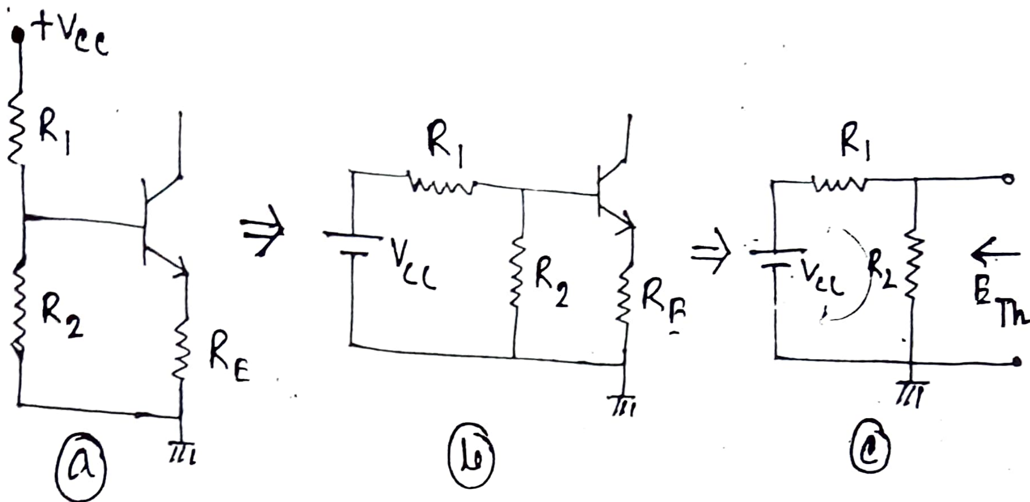
In approximate analysis we can calculate the value of I_C without depending upon β. This make the ckt more stable.



The ckt arrangement of voltage-divider bias is like that.

(1) Exact Analysis:

Input Side Ckt:



First calculate the total current in the loop shown in the fig (c).

$$I = \frac{V_{CC}}{R_1 + R_2}$$

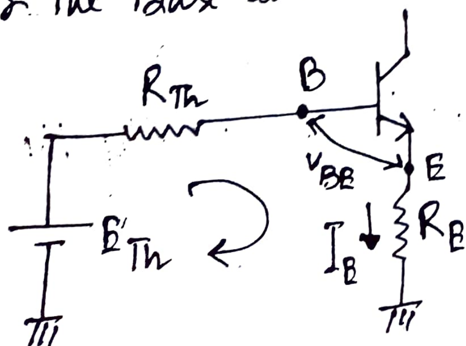
Next; Calculate the voltage across R_2 resistor and this voltage is known as Thevenin voltage (E_{Th} / V_{Th}).

$$E_{Th} = V_{Th} = V_{R_2} = IR_2 = \frac{R_2 V_{CC}}{R_1 + R_2}$$

[This is also known as voltage Divider rule]

And in this loop the equivalent Thevenin resistance is $R_{Th} = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2}$

Thus the Base-emitter loop can be drawn as follows:



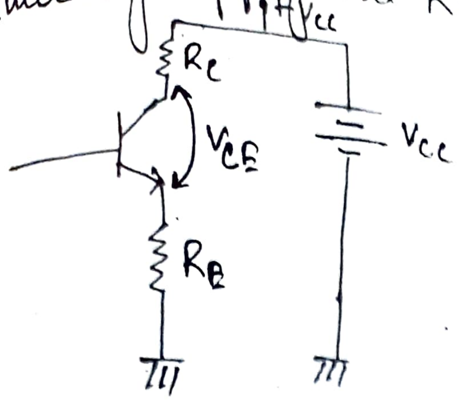
Apply KVL in the base emitter loop:

$$E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

$$\Rightarrow E_{Th} - I_B R_{Th} - V_{BE} - (1+\beta) I_B R_E = 0.$$

$$\Rightarrow \boxed{I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta+1) R_E}}$$

Similarly apply the KVL to the collector - Emitter loop



$I_B R_E + V_{CB} + I_C R_C - V_{CC} = 0$

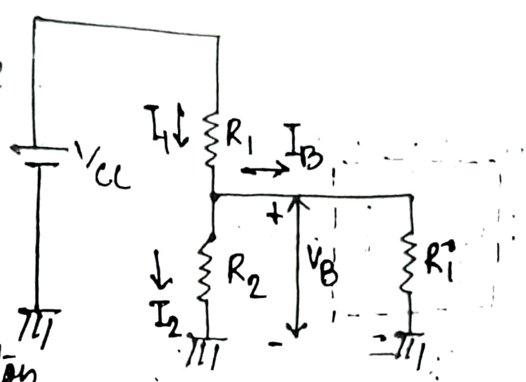
or, $V_{CB} = V_{CC} - I_C(R_C + R_E)$

$(\because I_C \cong I_B)$

Similarly we can determine the V_C, V_E and V_B as in the Emitter-Bias ckt.

② Approximate Analysis:

For approximate analysis we have to change the voltage divider bias ckt like that way. In this fig R_i is the equivalent resistance between base and ground for the transistor with an emitter resistor R_E and $R_i = (\beta+1)R_E$.



If $R_i >> R_2$ then all the current from V_{cc} will be diverted to R_2 rather flowing across R_i and I_2 will be approximately equal to I_1 and $I_B \cong 0$

Now the voltage across R_2 which is actually the bias voltage V_B is given by

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

Since $R_i = (\beta+1)R_E \cong \beta R_E$ the condition for approximate analysis is $\boxed{\beta R_E \geqslant 10 R_2}$

Once V_B is determined, the level of V_E can be calculated from

$$V_E = V_B - V_{BE}$$

And the Emitter current can be determined from

$$I_E = \frac{V_E}{R_E} \quad ; \text{ Again } I_C \cong I_E$$

The collector-to-emitter voltage is determined by

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Note in the sequence of calculation that β does not appear and I_B was not calculated. The Q-point is therefore independent of the value of β.

Load line:

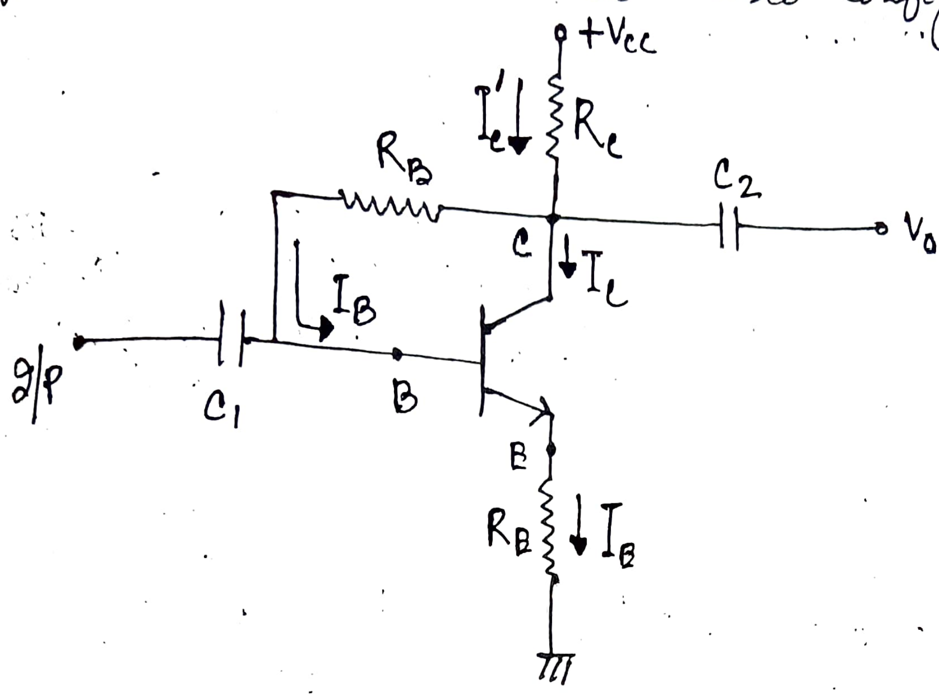
We have $V_{CE} = V_{CC} - I_C (R_C + R_E)$

When $V_{CE} = 0V$; $I_C = \frac{V_{CC}}{R_C + R_E} = I_{C(max)}$

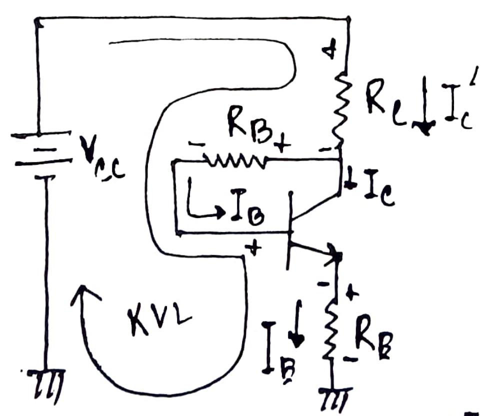
When $I_C = 0$; $V_{CE} = V_{CC} = V_{CE(max)}$

DC Bias With Voltage Feedback:

An improved level of stability can also be obtained by introducing a feedback path from collector to base. Although the Q-point is not totally independent of beta, but the sensitivity of changes in beta or temperature variations is normally less then for the fixed-bias or emitter-biased configuration.



Base-emitter loop:



$V_{cc} - I_c' R_c - I_B R_B - V_{BE} - I_E R_E = 0$

$\Rightarrow V_{cc} - I_c R_c - I_B R_B - V_{BE} - I_E R_E = 0$

$\left[\because I_c' = I_c + I_B \Rightarrow I_c' = I_c \ (\because I_B \simeq 0)\right]$

$\Rightarrow V_{cc} - \beta I_B R_c - I_B R_B - V_{BE} - \beta R_E I_B = 0$

$$\Rightarrow \boxed{I_B = \frac{V_{cc} - V_{BE}}{R_B + \beta(R_c + R_E)}}$$

Again $I_C = \beta I_B$

Collector-Emitter loop:

Applying KVL in this loop:

$$V_{CC} - I_C' R_C - V_{CE} - I_E R_E = 0$$

$$\Rightarrow V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Load line: The load line is same as for the voltage divider bias configuration.

STABILIZATION:

* The maintenance of the operating point stable (independent of temp variation or variations in transistor parameter) is known as stabilization.

* Stabilization is necessary due to the following reasons:

  (i) Temp. dependence of I_C

  (ii) Individual variations.

  (iii) Thermal runaway.

(Imp)

STABILITY FACTOR:

* I_C varies whenever there is variation in I_{CO}, β, & V_{BE}. Hence stability factor is defined as the rate of change of collector current I_C with any particular parameter i.e. I_{CO}, β, V_{BE}.

$$S(I_{CO}) = \frac{\partial I_C}{\partial I_{CO}}$$

$$S(\beta) = \frac{\partial I_C}{\partial \beta}$$

$$S(V_{BE}) = \frac{\partial I_C}{\partial V_{BE}}$$

Modelling :- A model is the combination of circuit elements, properly chosen, that approximates the actual behaviour of semiconductor device under specific operating conditions.

Types of Model :-

1. re model
2. hybrid model.

→ The ac equivalent of a network is obtained by

Step 1 setting all the dc sources to zero & replacing them by short circuit equivalent

Step 2 Removing all the capacitor by short circuit equivalent

Step 3 Redrawing the n/w in a more convenient & logical form.

Important Parameters :- (Z_i, Z_o, A_v, A_i)

input impedance,

$Z_i = \frac{V_i}{I_i}$

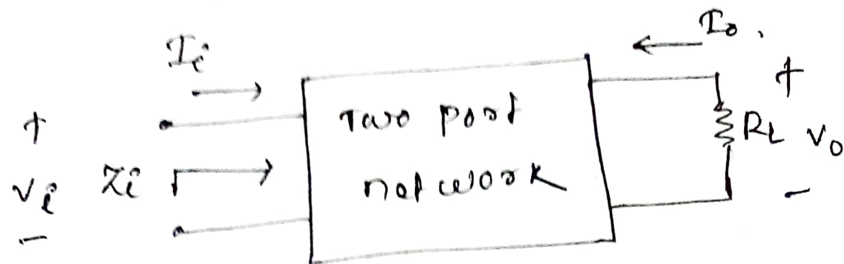
A_V (voltage gain) $= \frac{V_o}{V_i} \Big|$ under no load conditions

output impedance,

$Z_o = \frac{V_o}{I_o}$

$\left| A_{VNL} = \frac{V_o}{V_i} \right|$

→ The no load voltage gain for a transistor amplifier is always greater than the loaded voltage gain



$$A_i = \frac{I_o}{I_i}$$

$$I_o = -\frac{V_o}{R_L}$$

$$I_i = \frac{V_i}{Z_i}$$

$$A_i = \frac{I_o}{I_i} = \frac{-V_o/R_L}{V_i/Z_i}$$

$$= \frac{-V_o Z_i}{V_i R_L} = -\left(\frac{V_o}{V_i}\right) \cdot \frac{Z_i}{R_L} = -A_V \cdot \frac{Z_i}{R_L}$$

$$Z_i = \frac{V_i}{I_i}$$

$$Z_o = \frac{V_o}{I_o}$$

$$A_V = \frac{V_o}{V_i}$$

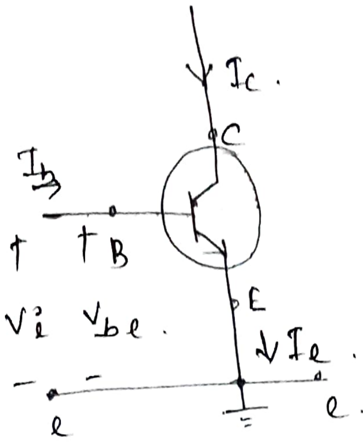
$$A_i = \frac{I_o}{I_i} = -A_V \frac{Z_i}{R_L} .$$

re transistor Model :- It employees a diode and controlled current source to duplicate the behaviour of a transistor.

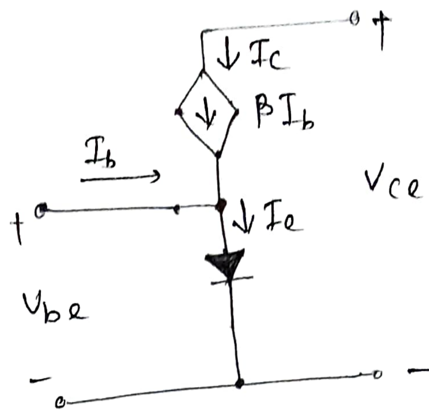
→ 3 types of re model are there.

1) common emitter configuration
2) common Base "
3) common collector "

Common Emitter configuration :-



I/p ckt for BJT.



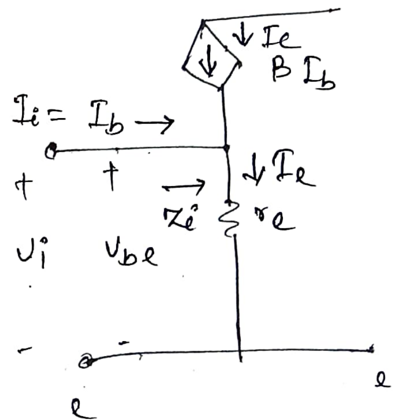
BJT equivalent ckt.

→ Replace the diode by its equivalent Resistance as determined by the level I_E.

Diode Resistance determined by $\boxed{r_D = \frac{26\,mV}{I_D}}$.

→ Using the subscript e, I_e is the emitter current

So $\boxed{r_e = \frac{26\,mV}{I_e}}$



Defining the level of Z_i.

→ For i/p side. $I_i = I_b$

$$Z_i = \frac{V_i}{I_b} = \frac{V_{be}}{I_b}$$

$$= \frac{I_e r_e}{I_b}$$

$$I_e = I_c + I_b$$

$$= \beta I_b + I_b$$

$$= I_b(\beta + 1)$$

$\boxed{I_e \simeq \beta I_b}$ sin ($\beta >> 1$)

so $\boxed{Z_i = \frac{\beta I_b r_e}{I_b} = \beta r_e}$

$Z_o = \infty$

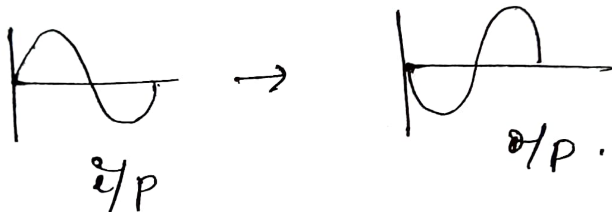
$$A_V = \frac{V_o}{V_i} = \frac{-I_o R_L}{I_e r_e} = \frac{-I_c R_L}{\beta I_b r_e}$$

$$= \frac{-\beta I_b R_L}{\beta I_b r_e}$$

$$\boxed{A_V = -\frac{R_L}{r_e}}$$

→ The -ve sign denotes that the output and input voltages are 180° out of phase.

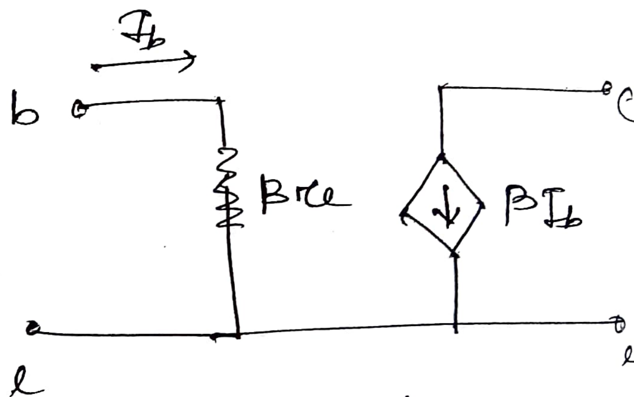
means



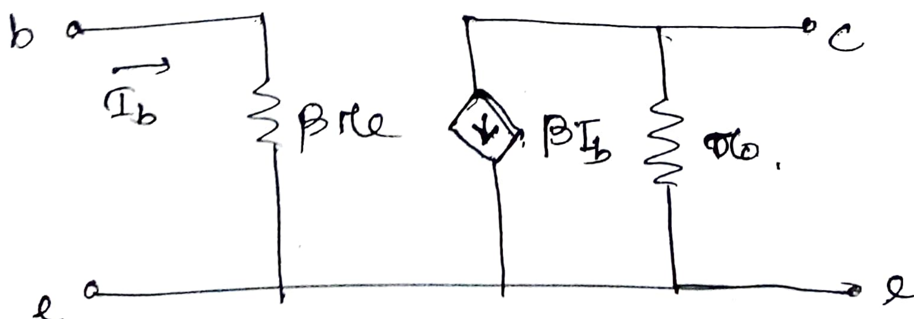
$$A_i = \frac{I_o}{I_i}$$

$$= \frac{I_c}{I_b} = \frac{\beta I_b}{I_b}.$$

$$\boxed{A_i = \beta}$$

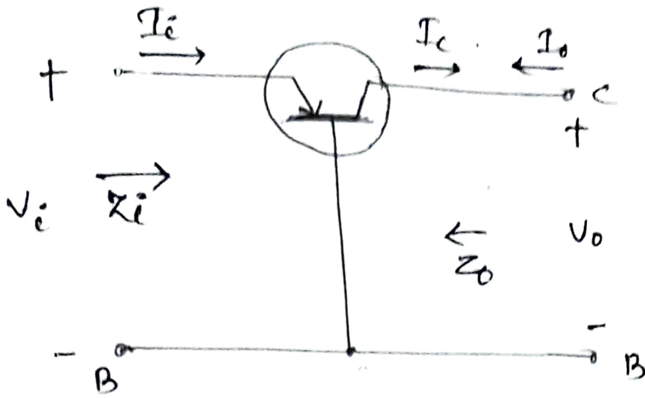


improved BJT eq Model.

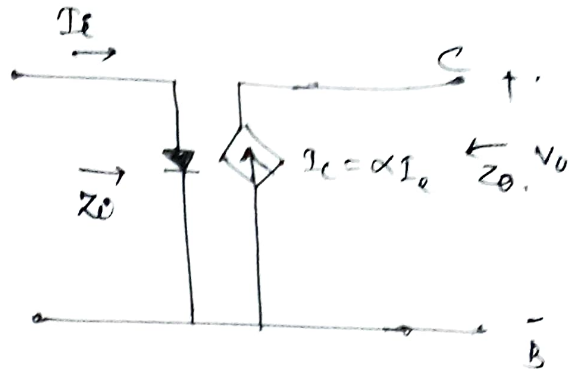


r_e model for the common-emitter transistor configuration including effect of r_o.

Common-Base configuration :-



a. (common Base BJT transistor)



b. equivalent

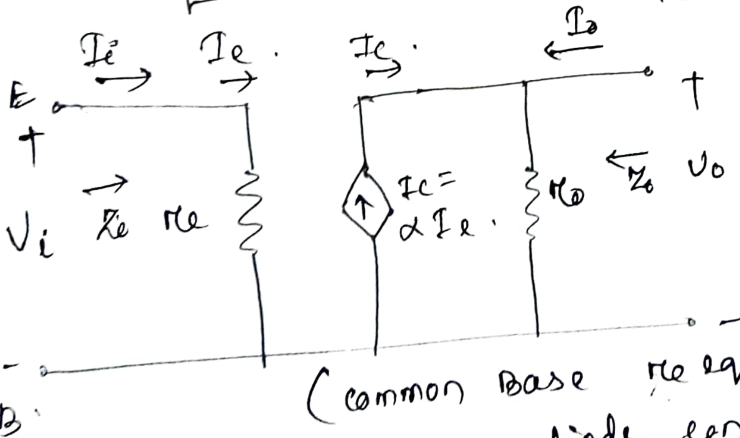
The a.c resistance of a diode is given by equation

$$r_{ac} = \frac{26\,mV}{I_D} \quad \text{--- (1)}$$

I_D = drain current through the diode or diode current.

$$\therefore \; r_e = \frac{26\,mV}{I_E} \quad \text{--- (2)}$$

where I_E is the d.c equivalent current at the emitter terminal.



(common Base r_e equivalent circuit)

→ For ac response, the diode can be replaced by its equivalent ac resistance determined by equation (2).

→ r_o is high.

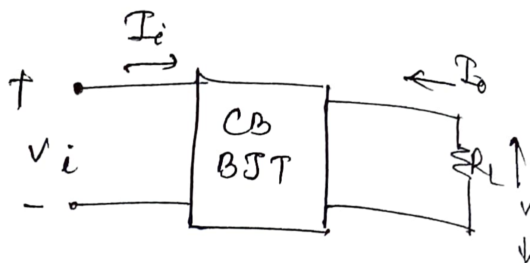
$Z_{in} = r_e$

$Z_o = \infty\,\Omega$

$A_V = \frac{V_o}{V_i}$

$V_o = -I_o R_L = -(-I_c) R_L$

$V_o = \alpha I_e \cdot R_L$



$V_i = I_i Z_i$

$V_i = I_e r_e$

$$A_V = \frac{V_o}{V_i} = \frac{\alpha I_e R_L}{I_e r_e}$$

$$A_V = \frac{\alpha R_L}{r_e}$$

$$A_V \simeq \frac{R_L}{r_e} \quad (\text{as } \alpha < 1)$$

$$A_i = \frac{I_o}{I_i} = \frac{-I_c}{I_e} = \frac{-\alpha I_e}{I_e} = -\alpha.$$

$$\boxed{A_i \simeq -1.}$$

Q) For a common base circuit $I_e = 4mA$, $\alpha = 0.98$. A signal of 2mV is applied between the base emitter terminals. Determine Z_i, A_V if a lo... of $0.56\,k\Omega$ is connected. Also find Z_o an...

Sol) $I_e = 4mA$

$\alpha = 0.98$

$V_i = 2mV.$

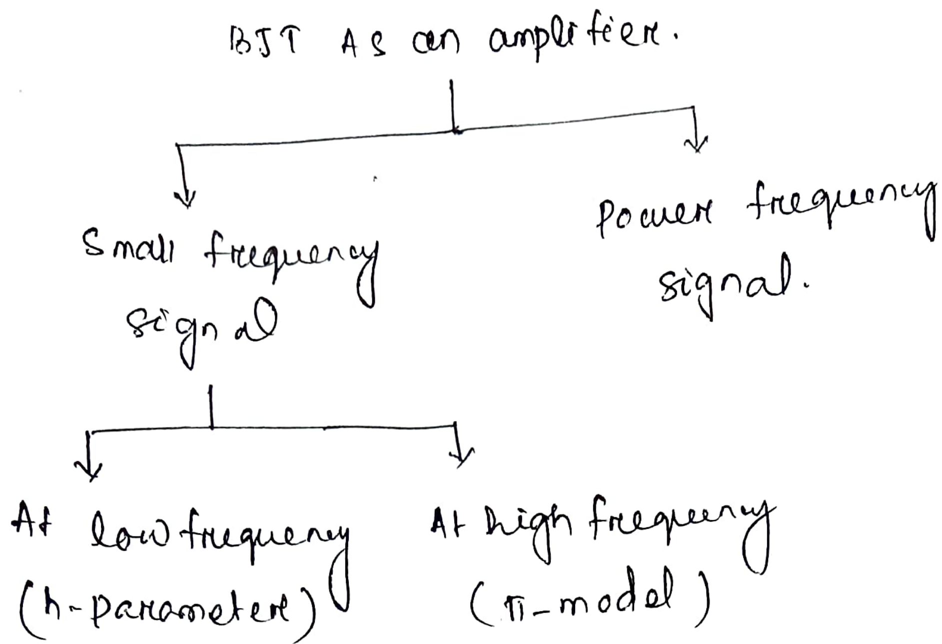
$$r_e = \frac{26\,mV}{I_e} = \frac{26\,mV}{4\,mA} = 6.5\,\Omega$$

$Z_i = r_e = 6.5\,\Omega$

$Z_o = \infty$

$$A_V = \frac{\alpha R_L}{r_e} = \frac{0.98 \times 0.56\,k\Omega}{6.5\,\Omega} = 84.4$$

$$A_i = \frac{-\alpha I_e}{I_e} = -0.98$$



⇒ Small frequency signal :-

1) Range of ac signal are μV to mV.
2) BJT must act in linear & active mode.
3) Magnitude of gain is important.
4) capacitance is negligible.

⇒ High frequency signal:-

1) BJT may operate in non-linear mode.
2) There must be impedance matching of device & load.
3) power level of o/p is an important parameter. Hence circuit efficiency is studied.
4) Diffusion capacitance (~~Studied~~) & transistion capacitance (CT) are exist due to high frequency.

⇒ Parameter of Amplifier :-

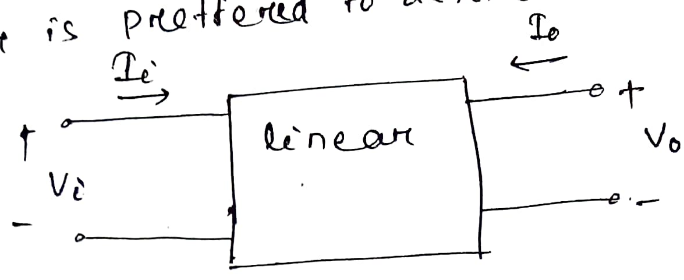
1) voltage gain (Av) 2) current gain (Ai) 3) input impedance (Zi) (4) output impedance (Zo)

Hybrid Parameters :-

→ The parameters relating the four variables are called h-parameters, from the word "hybrid".

→ The term hybrid was chosen because the mix of variables (V & I) in each equation results in a "hybrid" set of units of measurement for the h-parameters.

→ h-parameter is preferred to define a particular transistor at low frequency.



→ ~~If we set $V_o = 0$ and solve for h_{11}~~

$$\begin{vmatrix} V_i \\ I_o \end{vmatrix} = \begin{vmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{vmatrix} \begin{vmatrix} I_i \\ V_o \end{vmatrix}$$

$$V_i = h_{11} I_i + h_{12} V_o \quad \text{—— (1)}$$

$$I_o = h_{21} I_i + h_{22} V_o \quad \text{—— (2)}$$

If we arbitarily set $V_o = 0$ and solve for h_{11} eq^n (1), we find.

$$h_{11} = \left. \frac{V_i}{I_i} \right|_{V_o = 0} \text{ ohms.} \quad \text{when o/p s.c}$$

put $I_i = 0$,

$$h_{12} = \left. \frac{V_i}{V_o} \right|_{I_i = 0} \text{ unitless} \quad \text{when i/p o}$$

$V_o = 0$, by shorting the output terminals, the following result for h_{21}

$$h_{21} = \left. \frac{I_o}{I_i} \right|_{V_o = 0} \text{ unitless} \quad \text{when o/p is}$$

put $I_i = 0$.

$$h_{22} = \left. \frac{I_o}{V_o} \right|_{I_i = 0} \text{ siemens.}$$

when i/p is

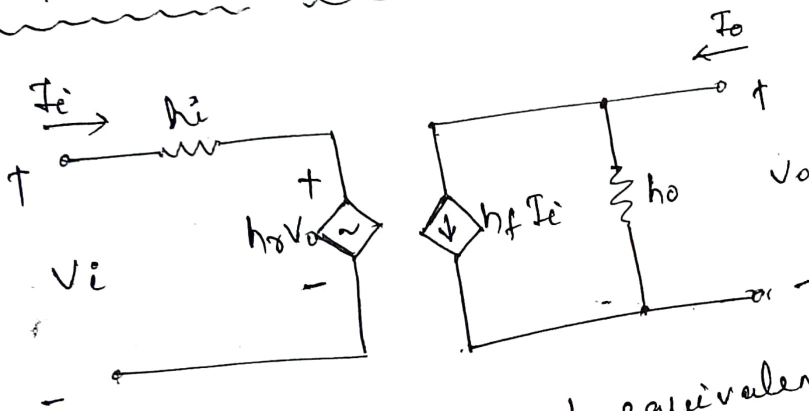
→ Hence h_{11} is called input impedance with output shorted.

→ Hence h_{21} is called forward current gain with o/p shorted.

→ h_{12} is called reverse voltage gain with circuit opened.

→ h_{22} is called output admittance with input terminal opened.

h-Parameter equivalent circuit :-



(complete hybrid equivalent circuit)

→ The i/p circuit appears as resistance h_i in series with voltage source $h_r V_o$.

→ The output circuit involves two component, a current source $h_f I_i$ and shunt resistance h_o.

→ The circuit is called hybrid equivalent because its input portion is thevenin's equivalent i.e voltage source with series resistance while output portion is norton equivalent. i.e current source with shunt resistance.

h-parameter	Notation in Common Base	Notation in common Emitter	Notation in common collector
h_{11}	h_{ib}	h_{ie}	h_{ic}
h_{12}	h_{rb}	h_{re}	h_{rc}
h_{21}	h_{fb}	h_{fe}	h_{fc}
h_{22}	h_{ob}	h_{oe}	h_{oc}

$h_{11} \rightarrow$ I/p resistance $\rightarrow h_i$

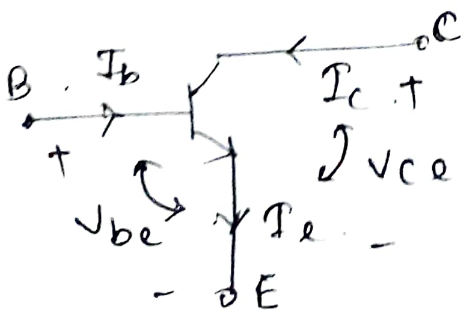
$h_{12} \rightarrow$ Reverse transfer voltage ratio $\rightarrow h_r$

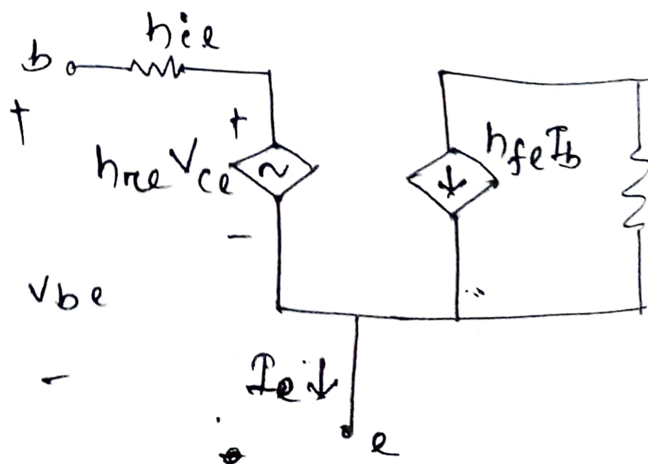
$h_{21} \rightarrow$ forward transfer current ratio $\rightarrow h_f$

$h_{22} \rightarrow$ output conductance $\rightarrow h_o$.

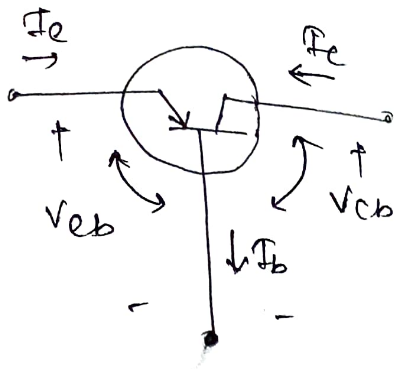
first subscript $\rightarrow$ the type of hybrid parameter
2nd " $\rightarrow$ the type of transistor connection

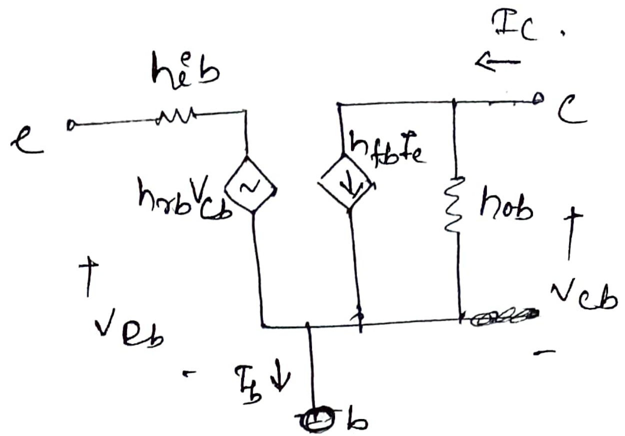
Hybrid Model (For common Emitter circuit)



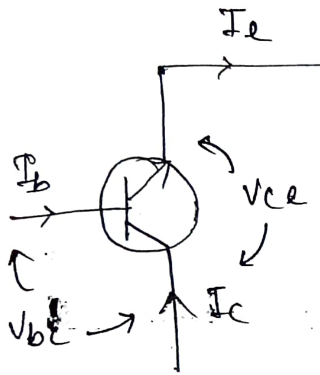


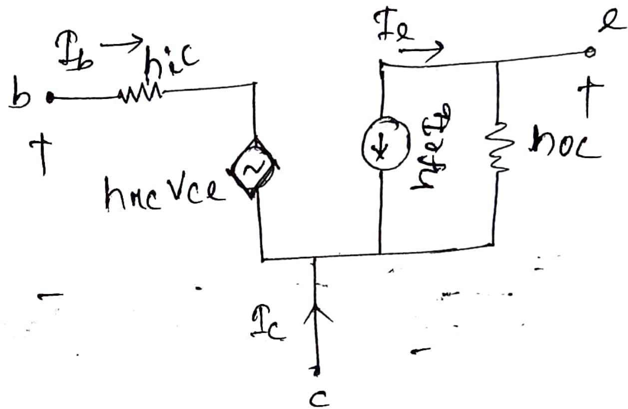
Hybrid Model for (common Base circuit)





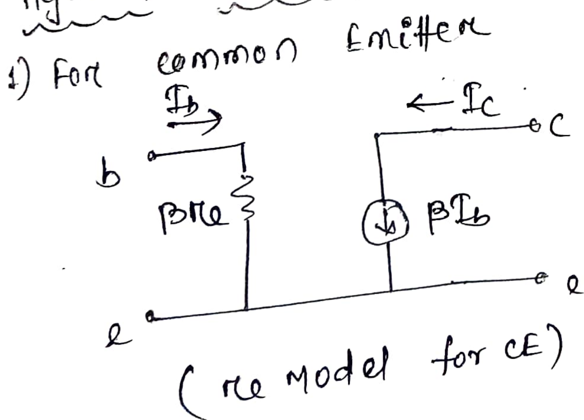
Hybrid Model for (common collector circuit)



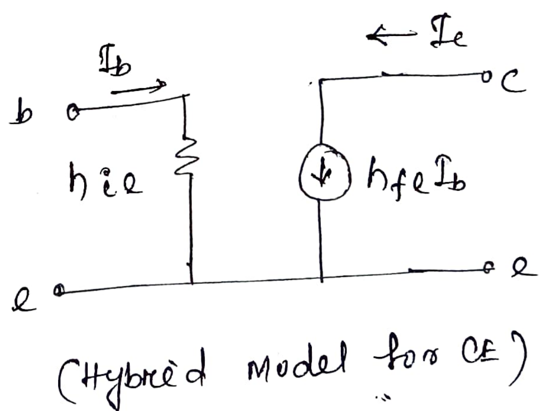


Hybrid Vs re Model.

1) For common Emitter



(re Model for CE)



(Hybrid Model for CE)

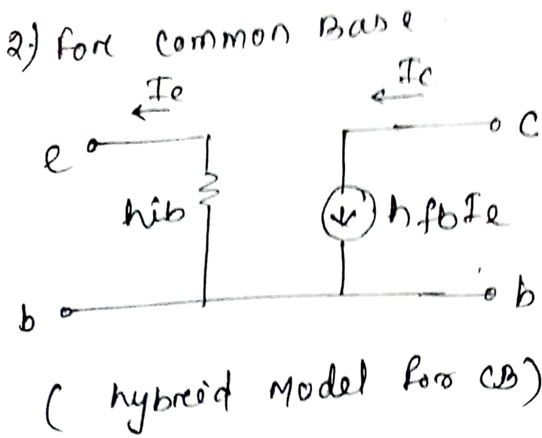
$$h_{ie} = \beta r_e$$

$$h_{fe} I_b = \beta I_b$$

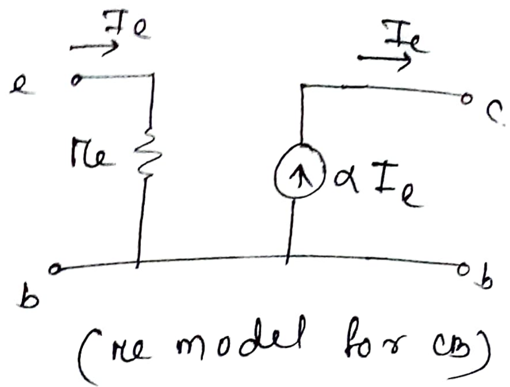
$$h_{fe} = \beta$$

$$r_o = \frac{1}{h_{oe}}$$

2) For common Base



(hybrid Model for CB)



(re model for CB)

$$h_{ib} = r_e$$

$$h_{fb} I_e = \alpha I_e .$$

$$h_{fb} = \alpha$$

Q Given $I_e = 2.5mA$
$h_{fe} = 140$.
$h_{oe} = 20\mu$siemen
$h_{ob} = 0.5\mu s$

Determine common emitter hybrid equivalent circuit and common base re model.

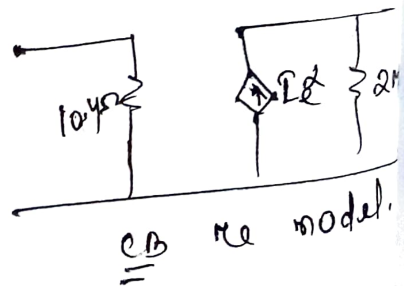
Sol a) $r_e = \dfrac{26mV}{I_e} = 10.4\Omega$

$h_{ie} = \beta r_e$
$= 140 \times 10.4$
$= 1.4 K\Omega$

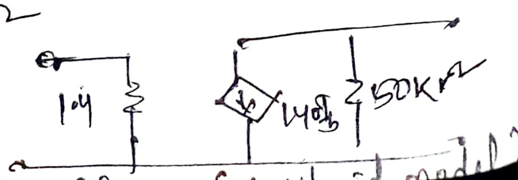
$h_{fe} = \beta$

$r_o = \dfrac{1}{h_{oe}}$
$= \dfrac{1}{20\mu s}$
$= \dfrac{1}{20\times10^{-6}s} = 5\times10^{4}\Omega$
$= 50K\Omega$

b) $r_e = 10.4\Omega$
$\alpha \cong 1$,
$r_o = \dfrac{1}{h_{ob}} = \dfrac{1}{0.5\mu}$
$= 2M\Omega$

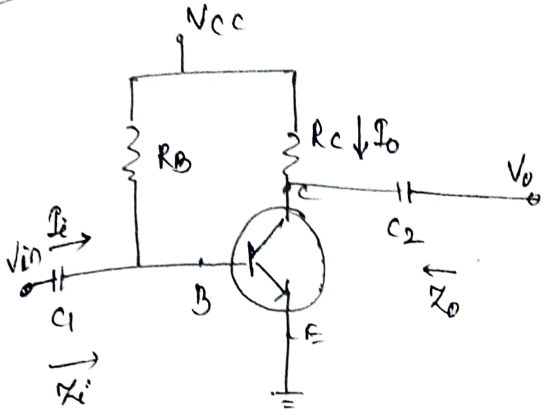


CB re model.

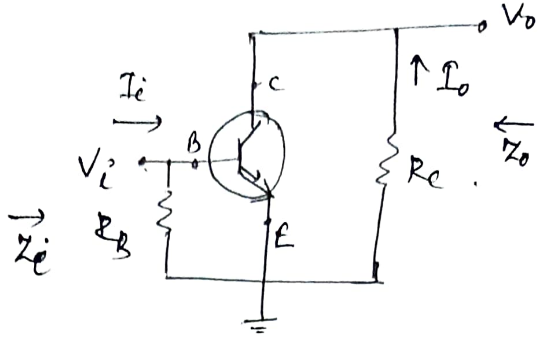


SMALL SIGNAL ANALYSIS OF CC, CE, CB

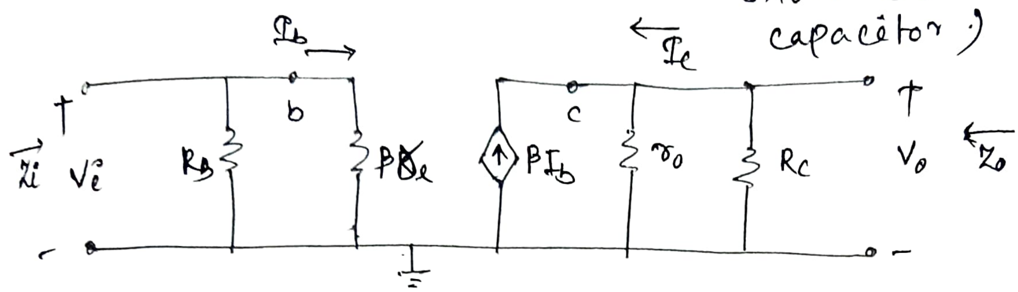
COMMON EMITTER FIXED BIAS CONFIGURATION :-



(Fixed Biased circuit)



(Removal of dc source & short circuiting the capacitor)



(re model)

$$\boxed{Z_i = R_B \parallel \beta r_e} \text{ ohms}$$

$$\boxed{Z_i \cong \beta r_e} \quad R_B \geq 10\beta r_e \text{ ohms}$$

→ If two resistances are taken in parallel and one of them is much larger than the other then the equivalent resistance is equal to the smaller value.

→ Z_o (Put $V_i = 0$, $I_b = 0$, current source is open circuit)

$$\boxed{Z_o = r_o \parallel R_C} \text{ ohms}$$

→ If $r_o \geq 10 R_C$, then $R_C \parallel r_o \cong R_C$ &

$$\boxed{Z_o \cong R_C} \quad r_o \geq 10 R_C.$$

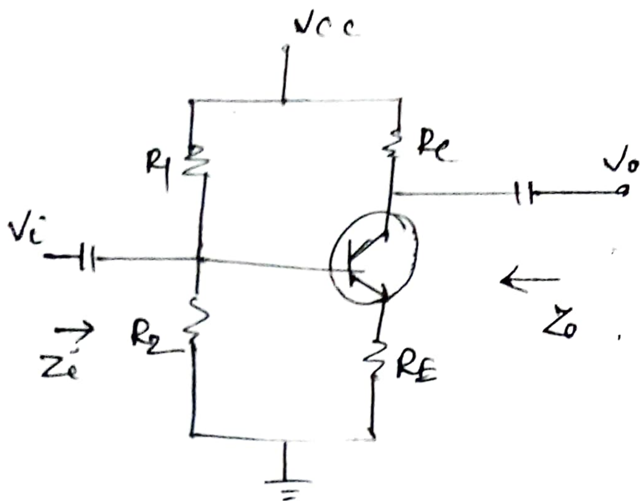
→ $V_o = -I_c Z_o$

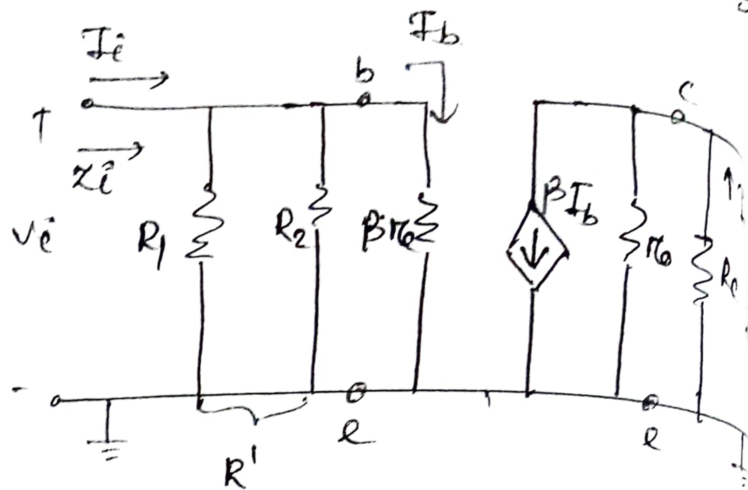
$= -\beta I_b (r_o \parallel R_C)$

$= -\beta \left(\frac{V_i}{\beta r_e}\right) \cdot (r_o \parallel R_C)$

$= \frac{-V_i}{} (r_o \parallel R_C)$

Voltage divider Bias





$Z_i = R_1 \parallel R_2 \parallel \beta r_e$

Let $R' = R_1 \parallel R_2$, then $\boxed{Z_i = R' \parallel \beta r_e}$

$Z_o = R_c \parallel r_o$ If $r_o \geq 10 R_c$, then $\boxed{Z_o = R_c}$

A_v $\frac{V_o}{V_i}$ = $-I_o \times Z_o$ = $-I_c Z_o$ = $-\beta I_b Z_o$

$= -\beta I_b \times (R_c \parallel r_o)$

$\Rightarrow V_o = -\beta \cdot \frac{V_i}{\beta r_e} \times (R_c \parallel r_o)$

$\Rightarrow \frac{V_o}{V_i} = \frac{-(R_c \parallel r_o)}{r_e}$

or $\boxed{A_V = \frac{-(R_c \parallel r_o)}{r_e}}$

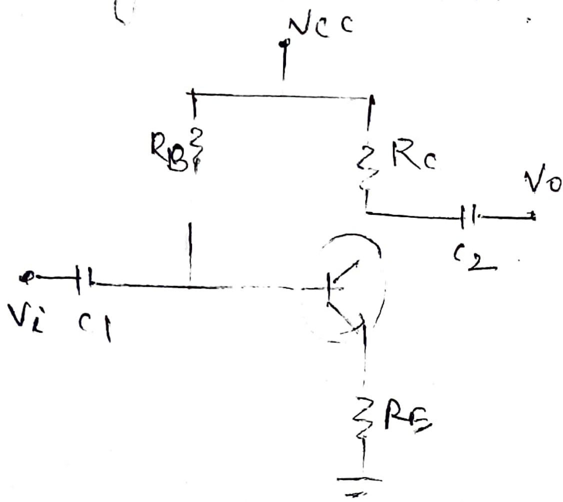
A_V is same as fixed Bias configuration.

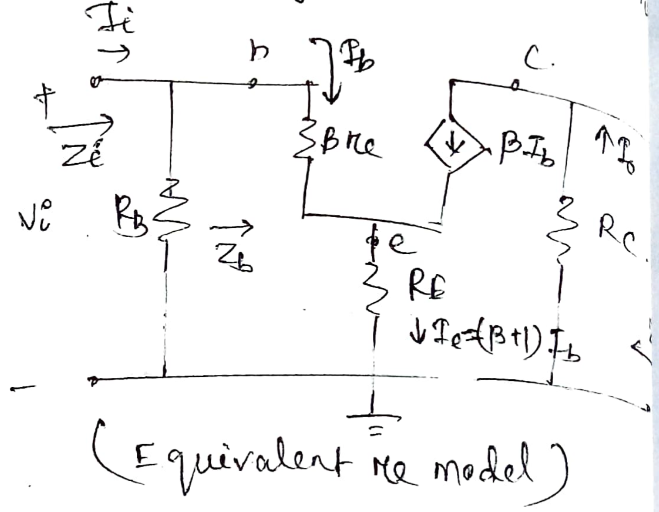
$\boxed{A_V = \frac{-R_c}{r_e}}$ $r_o \geq 10 R_c$.

Emitter-stabilized ckt / (CE Emitter-Bias configuration)

→ The emitter R_E may or may not be bypass in the ac domain. The effect of r_e is to make the analysis a great deal more complicated & in most situation its effect can be ignored. r_e is not in

1) Unbypassed





(Equivalent r_e model)

$$V_{in} = I_b \beta r_e + I_e R_E$$

$$= I_b \beta r_e + (\beta+1) I_b \cdot R_E$$

$$Z_b = \frac{V_i}{I_b} = \beta r_e + (\beta+1) R_E$$

→ The presence of R_E without CE affects the Z_i & A_v.

$$\boxed{Z_b = \beta(r_e + R_E)} \quad \text{if } \beta >> 1.$$

$$\boxed{Z_b = \beta R_E} \quad R_E >> r_e$$

$$\boxed{Z_i = R_B \| Z_b}$$ ✓ Z_i ↑ Z_o is higher compared to bypass capacitor

with $V_i = 0$, $I_b = 0$, βI_b can be replaced by open

$$\boxed{Z_o = R_C}$$ ✓ Z_o ↑ in presence of unbypassed emitter resistor

$$V_o = -I_o Z_o = -\beta I_b R_C = -\beta \cdot \frac{V_{in}}{Z_b} \cdot R_C$$

$$\frac{V_o}{V_{in}} = -\beta \frac{R_C}{Z_b} = \frac{-\beta R_C}{\beta(R_E + r_e)} = \frac{-\beta R_C}{\beta R_E} \quad R_E >> r_e$$

$$\boxed{A_V = \frac{-R_C}{R_E}} \quad (r_e << R_E)$$

or

$$\boxed{A_V = \frac{-R_C}{R_E + r_e}}$$ Voltage gain lowers

Effect of r_o

$$Z_b = \beta r_e + \left[\frac{(\beta+1) + (R_C/r_o)}{1 + (R_C + R_E)/r_o}\right] R_E \cong \beta(r_e + R_E) \Big|_{r_o \geq 10(R_C + R_E)}$$

$$Z_{in} = Z_b \parallel R_B$$

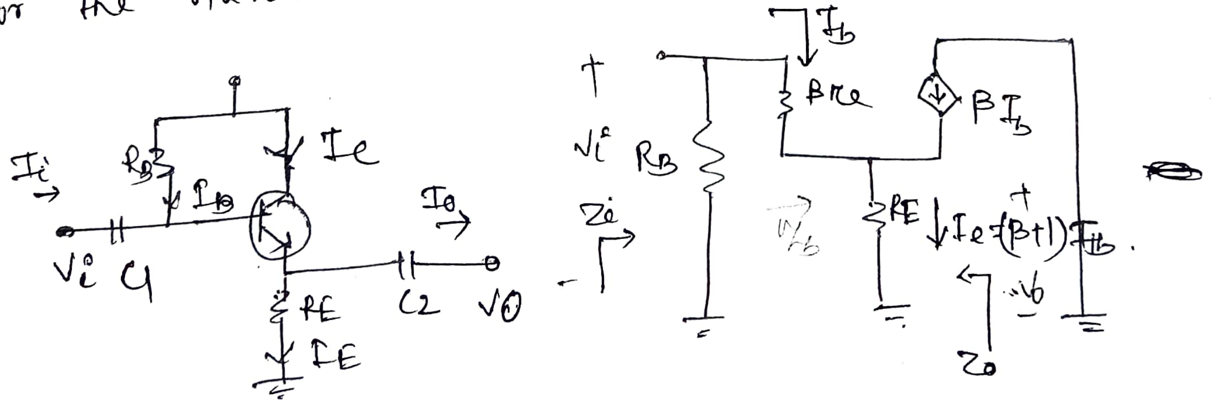
$$Z_o = R_C \parallel \left[r_o + \frac{\beta(r_o + r_e)}{1 + \frac{\beta r_e}{R_E}} \right] \cong R_C \Big|_{r_o >> r_e}$$

$$A_V = \frac{\frac{-\beta R_C}{Z_b}\left(1 + \frac{r_e}{r_o}\right) + \frac{R_C}{r_o}}{\left(1 + \frac{R_C}{r_o}\right)}$$

$$\boxed{A_V = \frac{-\beta R_C}{Z_b}} \quad r_o \geq 10 R_C$$

Emitter follower configuration :-

- when the o/p is taken from emitter terminal of the transistor, the n/w is referred to as a emitter follower.
- The emitter voltage is in phase with the i/p s/g v_i which means both o/p & i/p voltage attend their +ve & -ve peaks at the same time. The fact that v_o follows v_i with that inphase relationship accounts for the name emitter follower.



$$\boxed{Z_i = R_B \parallel Z_b}$$

$$Z_b = \beta r_e + (\beta+1) R_E$$

$$= \beta(r_e + R_E)$$

$$\boxed{Z_b \simeq \beta R_E} \quad R_E >> r_e$$

$$V_i = I_b \beta r_e + (\beta+1) I_b R_E$$

$$Z_b = \frac{V_i}{I_b} = \beta r_e + (\beta+1) R_E$$

$$\simeq \beta (r_e + R_E) . \quad (\because \beta+1 = \beta).$$

$$I_b = \frac{V_i}{Z_b}$$

$$I_e = (\beta+1) I_b = (\beta+1) \frac{V_i}{Z_b}$$

$$= \frac{(\beta+1) V_i}{\beta r_e + (\beta+1) R_E}$$

Devide $(\beta+1)$ in both numerator & denominator

$$I_e = \frac{V_i}{\left(\frac{\beta}{\beta+1}\right) r_e + R_E}$$

$$= \frac{V_i}{\frac{\beta}{\beta} r_e + R_E} \quad (\because \beta+1 \simeq \beta)$$

$$\boxed{I_e = \frac{V_i}{r_e + R_E}}$$

$$Z_o = r_e \parallel R_E$$

since $R_E >> r_e$

$$\boxed{Z_o = r_e}$$

A_V:-

$$V_o = \left(\frac{R_E}{R_E + r_e} \right) \times V_i$$

$$\frac{V_o}{V_i} = \frac{R_E}{R_E + r_e}$$

$$\boxed{A_V = \frac{R_E}{R_E + r_e}} \Rightarrow A_V = 1 \; \Big| \; r_e << R_E$$

Effect of r_o

$$Z_i = \beta r_e + \frac{(\beta+1) R_E}{1 + \frac{R_E}{r_o}}$$

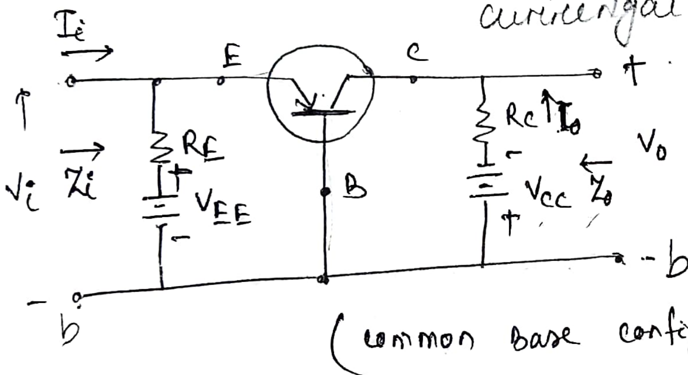
$$Z_o = r_o \parallel R_E \parallel \frac{\beta r_e}{\beta+1}$$

$$A_v = \frac{(\beta+1) R_E / Z_b}{1 + \frac{R_E}{r_o}}$$

$$\boxed{A_v = \frac{R_E}{r_e + R_E}} \quad r_o \geq 10 R_E$$

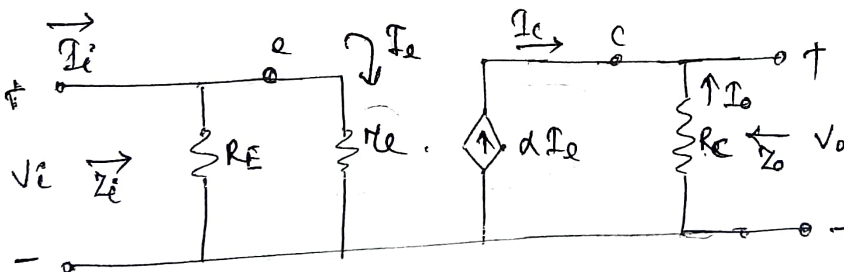
r_e model for common-Base configuration :-

low i/p impedance & high o/p impedance
current gain less than 1.

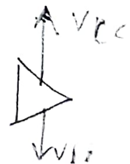


r_o (transistor o/p ...) is not included ... it is in terms of megaohm range & can be ignored ... with R_C

(common base configuration)



(r_e model)



$$\boxed{Z_i = R_E \parallel r_e}$$

If $R_E \geq 10 r_e$

$$\boxed{Z_i = r_e}$$

$$\boxed{Z_o = R_C}$$

$$V_o = -I_o Z_o = -(-I_c) \cdot R_C$$

$V_o = I_c R_c$

$= \alpha I_E R_c$

$= \alpha \cdot \frac{V_i}{r_e} \cdot R_c$

$$\frac{V_o}{V_i} = \frac{\alpha R_c}{r_e}$$

$$\boxed{A_v = \frac{\alpha R_c}{r_e}}$$

Current gain — $R_E >> r_e$, $I_i = I_E$

$Z_o = \frac{V_o}{I_o}$

$A_i = \frac{I_o}{I_i} = \frac{-I_c}{I_E}$ ($\because R_E >> r_e$, $I_i = I_E$)

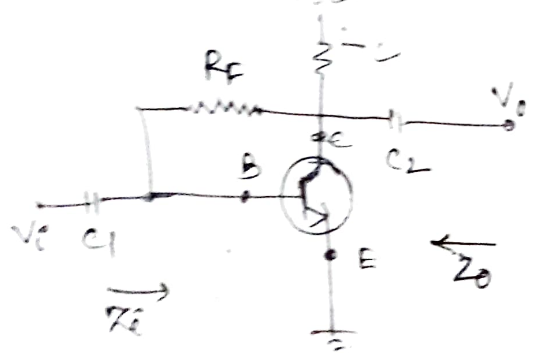
$= \frac{-\alpha I_E}{I_E}$

$$\boxed{A_i = -\alpha \simeq -1}$$

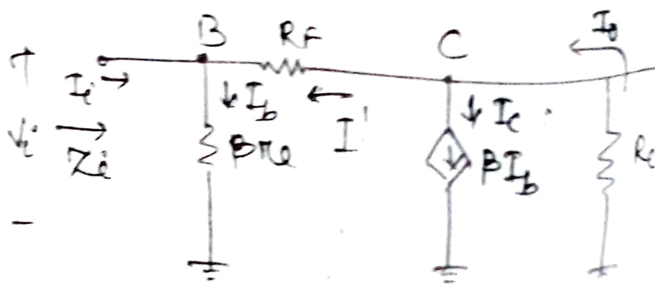
→ A_v is a positive number shows that V_o & V_i in phase for common-base configuration.

Collector Feedback Configuration :-

This circuit employes a feedback path from collector to base to increase the stability of the system.



(collector feedback configuration)



(r_e model)

$$I' = \frac{V_0 - V_i}{R_F}$$

$$V_0 = -I_0 R_C \quad \left\{ \because I_0 = \beta I_b + I' \cong \beta I_B \right\}$$
$$\cong -I_C R_C$$
$$V_0 = -\beta I_b R_C.$$

but $I_b = \frac{V_i}{\beta r_e}$.

$$V_0 = -\beta \left(\frac{V_i}{\beta r_e} \right) \cdot R_C$$
$$= -\frac{R_C}{r_e} \cdot V_i$$

$$\boxed{A_V = \frac{V_0}{V_i} = -\frac{R_C}{r_e}}$$

$$I' = \frac{V_0 - V_i}{R_F} = \frac{V_0}{R_F} - \frac{V_i}{R_F}$$
$$= \frac{-R_C V_i}{r_e R_F} - \frac{V_i}{R_F}$$
$$= -\frac{1}{R_F}\left[1 + \frac{R_C}{r_e}\right] V_i$$

$$V_i = I_b \beta r_e = (I_i + I')\beta r_e = I_i \beta r_e + I' \beta r_e$$

$$\Rightarrow V_i = I_i \beta r_e + \left\{ -\frac{1}{R_F}\left[1 + \frac{R_C}{r_e}\right] V_i \right\} \beta r_e$$

$$\Rightarrow V_i + \left\{ \frac{1}{R_F}\left[1 + \frac{R_C}{r_e}\right] V_i \right\} \beta r_e = I_i \beta r_e$$

$$\Rightarrow V_i \left[1 + \frac{\beta r_e}{R_F}\left(1 + \frac{R_C}{r_e}\right) \right] = I_i \beta r_e$$

$$\Rightarrow \frac{V_i}{I_i} = \frac{\beta r_e}{1 + \frac{\beta r_e}{R_F}\left(1 + \frac{R_C}{r_e}\right)}$$

$$1 + \frac{R_C}{r_e} \cong \frac{R_C}{r_e}$$

$$\Rightarrow \frac{V_i}{I_i} = \frac{\beta r_e}{1 + \frac{\beta r_e}{R_F} \times \frac{R_C}{r_e}}$$

$$\boxed{Z_i = \frac{V_i}{I_i} = \frac{\beta r_e}{1 + \frac{\beta R_C}{R_F}}}$$

or $$Z_i = \frac{r_e}{1/\beta + R_C/R_F}$$

$$Z_o = R_C \| R_F$$

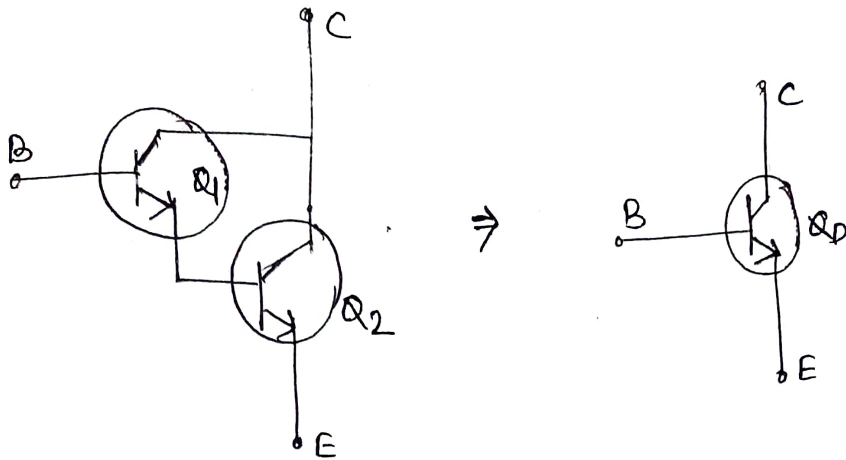
Effect of r_o

$$Z_i = \frac{1 + \frac{R_C \| r_o}{R_F}}{\frac{1}{\beta r_e} + \frac{1}{R_F} + \frac{R_C \| r_o}{R_F r_e}}$$

$$Z_o = r_o \| R_C \| R_F$$

$$A_V = \frac{-\left[\frac{1}{R_F} + \frac{1}{r_e}\right](r_o \| R_C)}{1 + \frac{r_o \| R_C}{R_F}}$$

Darlington Connection :-



(Darlington combination)

→ If two BJT are connected in such a way that they operated as an "superbeta" transistor, then that connection is known as Darlington connection.

→ If β_1 & β_2 are current gains, then darlington connection provide a current gain of

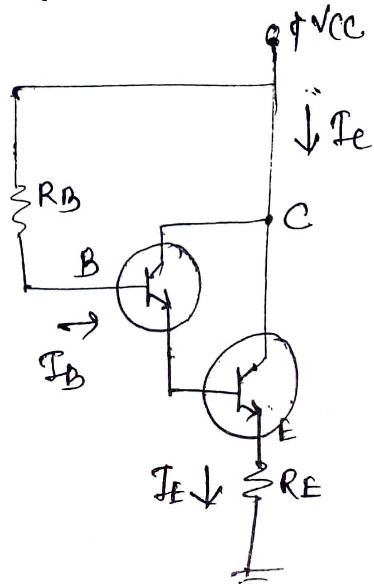
$$\boxed{\beta_D = \beta_1 \beta_2}$$

→ If the two transistors are matched so that $\beta_1 = \beta_2 = \beta$, the darlington connection provides a current gain of

$$\boxed{\beta_D = \beta^2}$$

→ A darlington transistor connection provides a transistor having a very large current gain, typically a few thousand.

DC Bias of darlington circuit :-



$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta_D R_E}}$$

β_D = high current gain

81

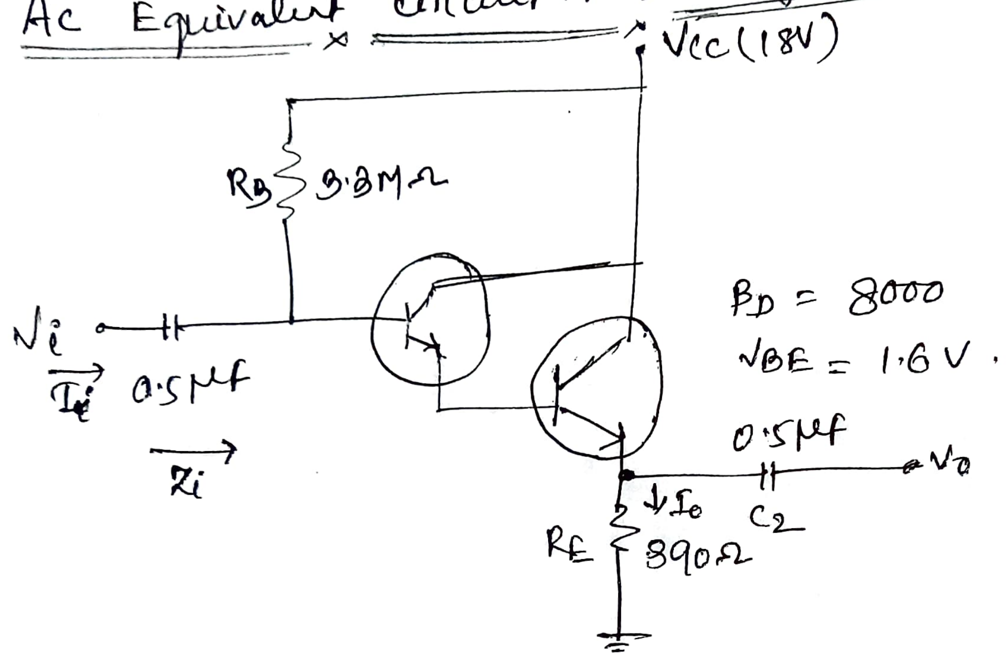
→ The value of β_D is much greater & the value of V_{BE} is larger.

$$I_E = (\beta_D + 1) I_B \approx \beta_D I_B$$

dc voltages are $V_E = I_E R_E$

$V_B = V_E + V_{BE}$

Ac Equivalent circuit of Darlington connection



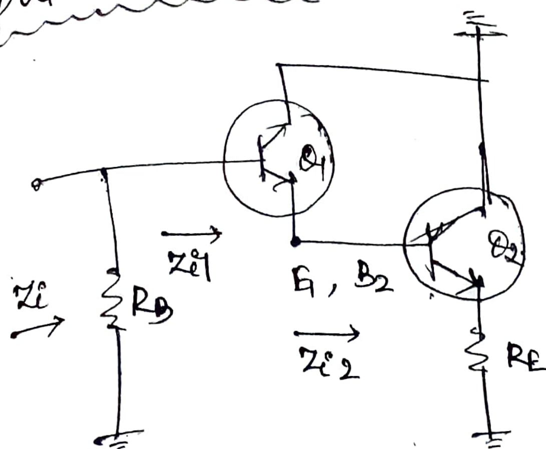
(Darlington Emitter follower circuit)

→ ac i/p sig is applied to Base of transistor through capacitor C_1.

→ ac o/p sig V_o obtained from emitter through capacitor C_2.

→ Due to the absence of a load R_L, the o/p current I_o is defined through R_E.

Input impedance.



(finding Z_i)

$$Z_{i2} = \beta_2 (r_{e2} + R_E)$$

$$Z_{i1} = \beta_1 (r_{e1} + Z_{i2})$$

$$Z_{i1} = \beta_1 (r_{e1} + \beta_2 (r_{e2} + R_E))$$

$$R_E >> r_{e2}$$

$$Z_{i1} = \beta_1 (r_{e1} + \beta_2 R_E)$$

$$\beta_2 R_E >> r_{e1}$$

$$Z_{i1} \cong \beta_1 \beta_2 R_E$$

$$= R_B \parallel Z_i$$

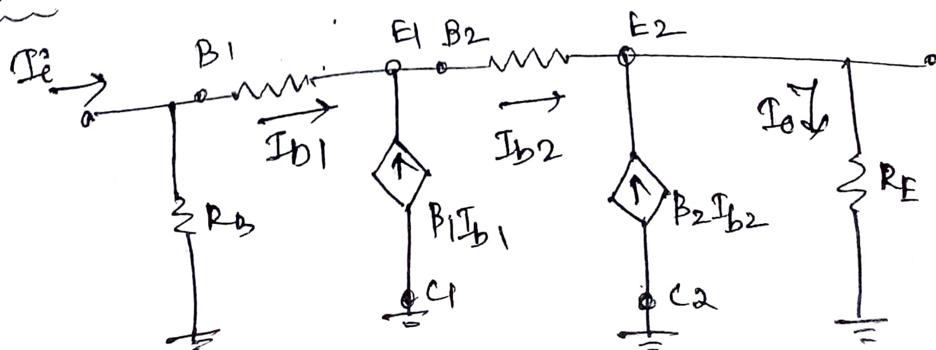
$$\boxed{Z_i = R_B \parallel \beta_1 \beta_2 R_E}$$

$$\beta_1 = \beta_2 = \beta$$

$$Z_i = R_B \parallel \beta^2 R_E$$

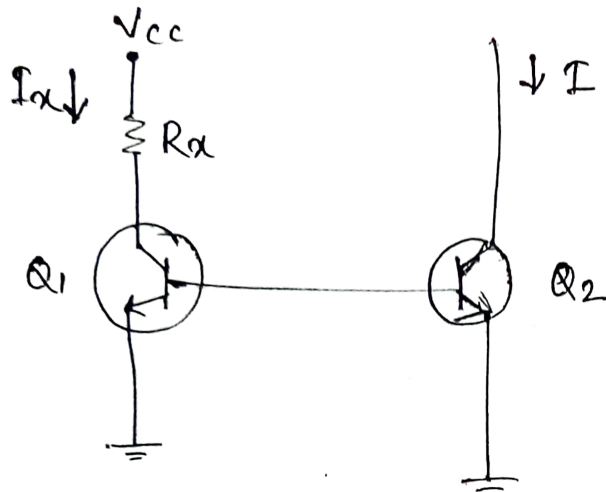
$$= R_B \parallel \beta_D R_E \quad (\because \beta_D = \beta_1 \beta_2)$$

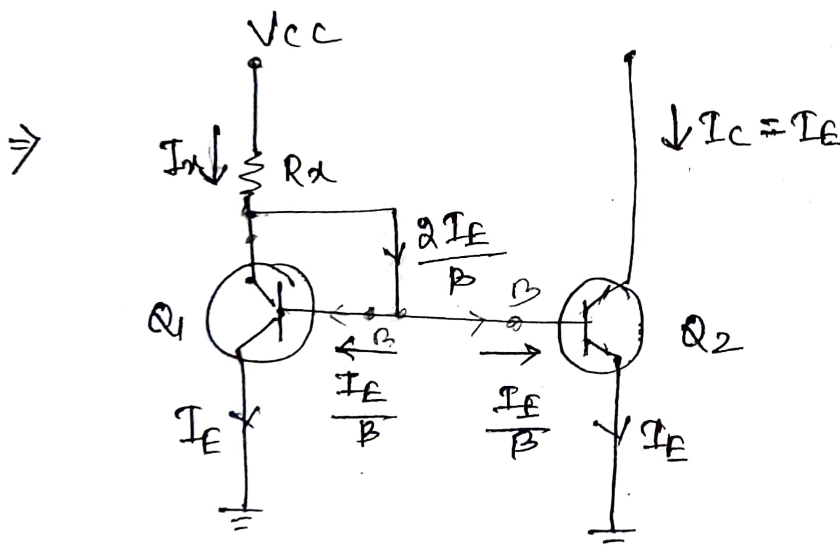
Current Gain :-



Current mirror circuits :-

- This circuit provides a constant current and is generally used in integrated circuit. This current is obtained from an output current is the reflection or mirror image of a current develop on the other side of circuit





$$I_E = (\beta+1) I_B$$

$$\simeq \beta I_B$$

$$I_x = \frac{V_{CC} - V_{BE}}{R_x}$$

$$\Rightarrow I_B = \frac{I_E}{\beta}$$

$$I_x = I_E + \frac{2I_E}{\beta} = I_E(1 + 2/\beta)$$

$$= \left(\frac{\beta+2}{\beta}\right) I_E = I_E\left(\frac{\beta+2}{\beta}\right)$$

$$\simeq I_E$$

(Assumption → emitter current of both the transistor